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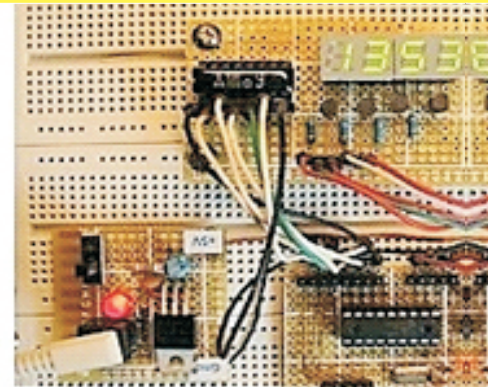
Name _____

Roll No. _____ Year 20 _____ 20 _____

Exam Seat No. _____

ELECTRONICS GROUP | SEMESTER - III | DIPLOMA IN ENGINEERING AND TECHNOLOGY

**A LABORATORY MANUAL
FOR
DIGITAL
TECHNIQUES
(22320)**



MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION, MUMBAI
(Autonomous) (ISO 9001 : 2015) (ISO / IEC 27001 : 2013)

VISION

To ensure that the Diploma level Technical Education constantly matches the latest requirements of technology and industry and includes the all-round personal development of students including social concerns and to become globally competitive, technology led organization.

MISSION

To provide high quality technical and managerial manpower, information and consultancy services to the industry and community to enable the industry and community to face the changing technological and environmental challenges.

QUALITY POLICY

We, at MSBTE are committed to offer the best in class academic services to the students and institutes to enhance the delight of industry and society. This will be achieved through continual improvement in management practices adopted in the process of curriculum design, development, implementation, evaluation and monitoring system along with adequate faculty development programmes.

CORE VALUES

MSBTE believes in the followings:

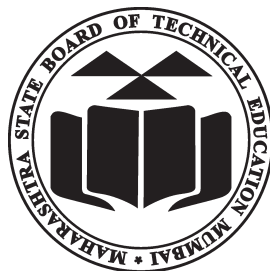
- Education industry produces live products.
- Market requirements do not wait for curriculum changes.
- Question paper is the reflector of academic standards of educational organization.
- Well designed curriculum needs effective implementation too.
- Competency based curriculum is the backbone of need based program.
- Technical skills do need support of life skills.
- Best teachers are the national assets.
- Effective teaching learning process is impossible without learning resources.

A Laboratory Manual
for
Digital Techniques

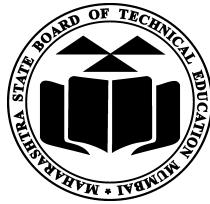
(22320)

Semester-III

(DE/EJ/ET/EN/EX/EQ/IE/IS/IC/MU/CO/CM/CW)

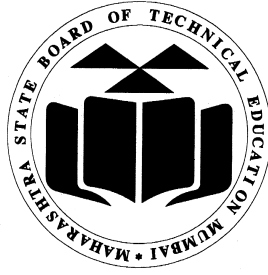


Maharashtra State
Board of Technical Education, Mumbai
(Autonomous) (ISO:9001:2015) (ISO/IEC 27001:2013)



Maharashtra State Board of Technical Education,
(Autonomous) (ISO:9001 : 2015) (ISO/IEC 27001 : 2013)
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Bandra (East), Mumbai - 400051.

(Printed on June, 2018)



**MAHARASHTRA STATE
BOARD OF TECHNICAL EDUCATION**

Certificate

This is to certify that Mr. / Ms.
Roll No., of Third Semester of Diploma in
..... of Institute,
.....

(Code:) has completed the term work satisfactorily in course
Digital Technique (22320) for the academic year 20..... to 20..... as
prescribed in the curriculum.

Place:

Enrollment No:.....

Date:

Exam. Seat No:

Subject Teacher

Head of the Department

Principal



Preface

The primary focus of any engineering laboratory/ field work in the technical education system is to develop the much needed industry relevant competencies and skills. With this in view, MSBTE embarked on this innovative ‘I’ Scheme curricula for engineering diploma programmes with outcome-base education as the focus and accordingly, relatively large amount of time is allotted for the practical work. This displays the great importance of laboratory work making each teacher; instructor and student to realize that every minute of the laboratory time need to be effectively utilized to develop these outcomes, rather than doing other mundane activities. Therefore, for the successful implementation of this outcome-based curriculum, every practical has been designed to serve as a ‘*vehicle*’ to develop this industry identified competency in every student. The practical skills are difficult to develop through ‘chalk and duster’ activity in the classroom situation. Accordingly, the ‘I’ scheme laboratory manual development team designed the practical to *focus* on the *outcomes*, rather than the traditional age old practice of conducting practicals to ‘verify the theory’ (which may become a byproduct along the way).

This laboratory manual is designed to help all stakeholders, especially the students, teachers and instructors to develop in the student the pre-determined outcomes. It is expected from each student that at least a day in advance, they have to thoroughly read through the concerned practical procedure that they will do the next day and understand the minimum theoretical background associated with the practical. Every practical in this manual begins by identifying the competency, industry relevant skills, course outcomes and practical outcomes which serve as a key focal point for doing the practical. The students will then become aware about the skills they will achieve through procedure shown there and necessary precautions to be taken, which will help them to apply in solving real-world problems in their professional life.

This manual also provides guidelines to teachers and instructors to effectively facilitate student-centered lab activities through each practical exercise by arranging and managing necessary resources in order that the students follow the procedures and precautions systematically ensuring the achievement of outcomes in the students.

In the present scenario most of the electronic equipment like computers, mobiles, music systems, ATM, automation and control circuits and systems are based on digital circuits which the diploma electronic engineering pass outs have to test them. The knowledge of basic logic gates, combinational and sequential logic circuits using discrete gates as well as digital ICs will enable the students to interpret the working of equipment and maintain them. After completion of the course, students will be able to develop digital circuits based applications.

Although best possible care has been taken to check for errors (if any) in this laboratory manual, perfection may elude us as this is the first edition of this manual. Any errors and suggestions for improvement are solicited and highly welcome

Programme Outcomes (POs) to be achieved through Practical of this Course:-

- PO1. **Basic knowledge:** Apply knowledge of basic mathematics, sciences and basic engineering to solve the broad-based Electronics and Computer engineering problems.
- PO2. **Discipline knowledge:** Apply Electronics and Computer engineering knowledge to solve broad-based Electronics and Computers engineering related problems.
- PO3. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Telecommunication engineering problems.
- PO4. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.
- PO5. **The engineer and society:** Assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to practice in field of Electronics and Telecommunication engineering.
- PO6. **Environment and sustainability:** Apply Electronics and Telecommunication engineering solutions also for sustainable development practices in societal and environmental contexts.
- PO7. **Ethics:** Apply ethical principles for commitment to professional ethics, responsibilities and norms of the practice also in the field of Electronics and Telecommunication engineering.
- PO8. **Individual and team work:** Function effectively as a leader and team member in diverse/ multidisciplinary teams.
- PO9. **Communication:** Communicate effectively in oral and written form.
- PO10. **Life-long learning:** Engage in independent and life-long learning activities in the context of technological changes also in the Electronics and Telecommunication engineering and allied industry.

Practical- Course Outcome matrix

Course Outcomes (COs)						
a Use number system and codes for interpreting working of digital system. b Use Boolean expressions to realize logic circuits. c Build simple combinational circuits. d Build simple sequential circuits. e Test data converters and PLDs in digital electronics systems.						
S. No.	Practical Outcome	CO a	CO b	CO c	CO d	CO e.
1	Test the functionality of specified logic gates using breadboard. (IC 7404, 7408, 7432, 7486)	-	√	-	-	-
2	Test the functionality of NAND and NOR gate using breadboard (IC 7400 and 7402)	-	√	-	-	-
3	Construct AND, OR, NOT gates using universal gates.	-	√	-	-	-
4	Build the logic circuit on breadboard to check the De Morgan's theorems.	-	√	-	-	-
5	Design Half adder and Half subtractor using Boolean expressions.	-	-	√	-	-
6	Design Full adder and full subtractor.	-	-	√	-	-
7	Construct and test BCD to 7 segment decoder using IC 7447/ 7448.	-	-	√	-	-
8	Build / test function of MUX 74151/74150/any other equivalent.	-	-	√	-	-
9	Build / test function of DEMUX 74155/74154/ any other equivalent.	-	-	√	-	-
10	Build / test function of RS flip flop using NAND Gate.	-	-	-	√	-
11	Build / test function of MS JK flip flop using 7476.	-	-	-	√	-
12	Use IC 7476 to construct and test the functionality of D and T flip flop.	-	-	-	√	-
13	Build/Testt 4 bit ripple counter using 7476.	-	-	-	√	-
14	Use IC 7490 to construct decade counter (MOD-10).	-	-	-	√	-
15	Build/test 4 bit universal shift register.	-	-	-	√	-
16	Build R-2R resistive network on breadboard to convert given digital data into analog.	-	-	-	-	√

List of Industry Relevant Skills

The following industry relevant skills of the competency '**Build/ test digital logic circuits consist of digital ICs.**' are expected to be developed in you by undertaking the practicals of this laboratory manual.

1. Identify the electronic IC / component.
2. Identify pin configuration for gates.
3. Test electronic IC / component.
4. Select the electronic component of proper value as per the requirement.
5. Select the appropriate range and instrument.
6. Mount the electronic component on breadboard as per circuit diagram.
7. Test the circuit for the given application.
8. Implement given Boolean equation using logic gates.
9. Use appropriate digital circuit.
10. Compare the observed output with the expected output.

Guidelines to Teachers

1. Teacher should provide the guideline with demonstration of practical to the students with all features.
2. Teacher shall explain prior concepts to the students before starting of each practical
3. Involve students in performance of each experiment.
4. Teacher should ensure that the respective skills and competencies are developed in the students after the completion of the practical exercise.
5. Teachers should give opportunity to students for hands on experience after the demonstration.
6. Teacher is expected to share the skills and competencies to be developed in the students.
7. Teacher may provide additional knowledge and skills to the students even though not covered in the manual but are expected the students by the industry.
8. Finally give practical assignment and assess the performance of students based on task assigned to check whether it is as per the instructions.
9. If practical is in two parts -Part I and Part II it should be conducted in two weeks.
10. Teacher is expected to refer complete curriculum document and follow guidelines for implementation
11. For difficult practicals if required, teacher could provide the demonstration of the practical emphasizing of the skills which the student should achieve.
12. Teachers should give opportunity to students for hands-on after the demonstration.
13. Teachers should give opportunity to students for hands-on after the demonstration.
14. Assess the skill achievement of the students and COs of each unit

Instructions for Students

1. Listen carefully the lecture given by teacher about course, curriculum, learning structure, skills to be developed.
2. Organize the work in the group and make record of all observations.
3. Students shall develop maintenance skill as expected by industries.
4. Student shall attempt to develop related hand-on skills and gain confidence.
5. Student shall develop the habits of evolving more ideas, innovations, skills etc. those included in scope of manual
6. Student shall refer technical magazines, IS codes and data books.
7. Student should develop habit to submit the practical on date and time.
8. Student should well prepare while submitting write-up of exercise.

Content Page
List of Practicals and Progressive Assessment Sheet

S. No	Title of Practical	Page No.	Date of performance	Date of submission	Assessment marks(25)	Dated sign. of teacher	Remarks(if any)
1.	Test the Functionality of logic gates	1					
2.	Test the Functionality of Universal logic gates	8					
3.	Construct basic gates using universal gates.	15					
4.	Verify De Morgan's Theorems.	23					
5.	Design Half adder and Half Subtractor using Boolean expressions.	30					
6.	Design Full adder and full subtractor.	37					
7.	Construct and test BCD to 7 segment decoder using IC 7447/ 7448.	45					
8.	Verify operation of Multiplexer (MUX).	55					
9.	Functionality of Demultiplexer(DEMUX).	62					
10.	Test functionality of RS flip flop using NAND gate.	69					
11.	Test functionality of MS JK flip flop.	75					
12.	Test the functionality of D and T flip flop.	81					
13.	4 bit ripple counter	87					
14.	Decade counter using IC 7490.	94					
15.	4 bit universal shift register.	100					
16.	R-2R resistive network.	106					
Total							

- **To be transferred to Proforma of CIAAN-2017**

Practical No.1: Test the functionality of logic gates.

I Practical Significance

Logic gates are the basic building block of all type of digital systems. Digital gates are used in all digital circuits such as switches, memories, microprocessor, and embedded systems. Knowledge of functions of logic gates will help the students to build the digital circuits.

II Relevant Program Outcomes (POs)

- **Basic knowledge:** Apply knowledge of basic mathematics, sciences and basic engineering to solve the broad-based Electronics and Computer engineering problems.
- **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based electronics and telecommunication engineering related problems.
- **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
- **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency: ‘**Build/ test digital logic circuits using digital ICs.**’

1. Verify voltage level for logic 0 and 1.
2. Identify pin configuration of logic gate IC’s.
3. Test the functionality of the logic gates.

IV Relevant Course Outcome(s)

- Use Boolean expressions to realize logic circuits.

V Practical Outcome

- Test the functionality of specified logic gates using breadboard.
(IC 7404, 7408, 7432, 7486)

VI Relevant Affective domain related Outcome(s)

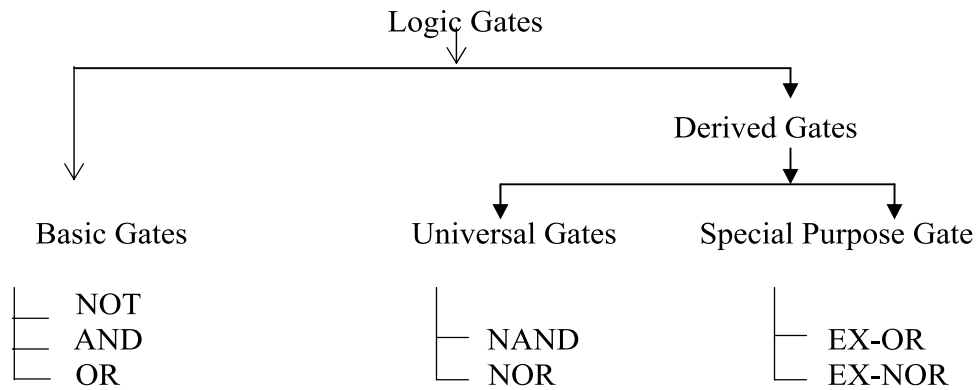
- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

A logic gate is an electronic circuit which makes logical decisions. It has only one output and one or many inputs. The output signal appears for certain combinations of input signals. Logic gates are the basic building blocks of all digital systems. These gates are AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the help of truth tables.

In digital logic design only two voltage levels or states are applied as input, and these states are generally referred to as Logic “1” and Logic “0”, High and Low, or True and False. These two states are represented in truth tables as binary digits “1” and “0” respectively.

Classification of Logic Gates:-



VIII Practical Circuit diagram

a) Sample

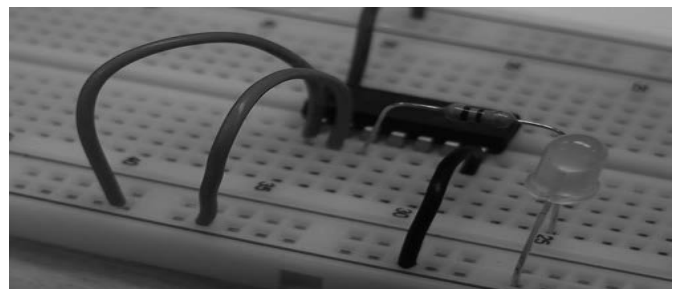
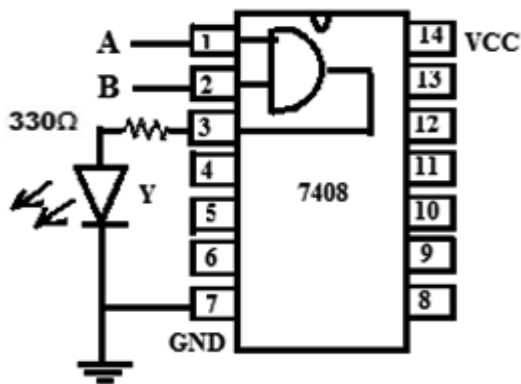


Figure 1.1: Sample Circuit

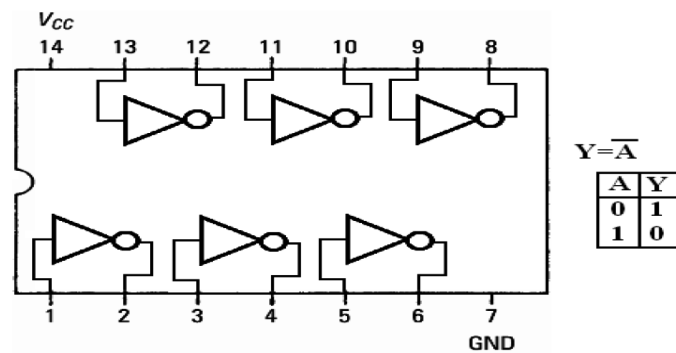


Figure 1.2 NOT Gate IC 7404 and truth table

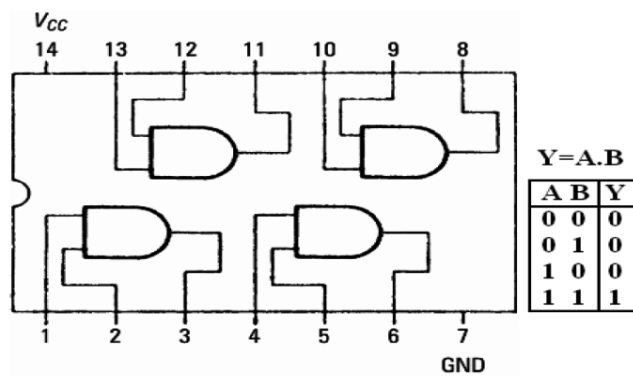


Figure 1.3 AND gate IC 7408 and truth table

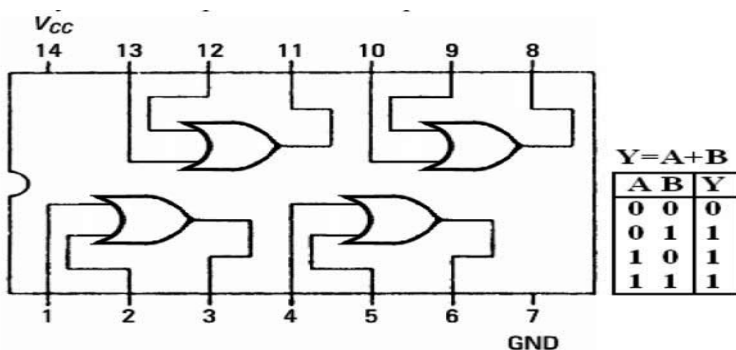


Figure 1.4. OR Gate IC 7432 and truth table

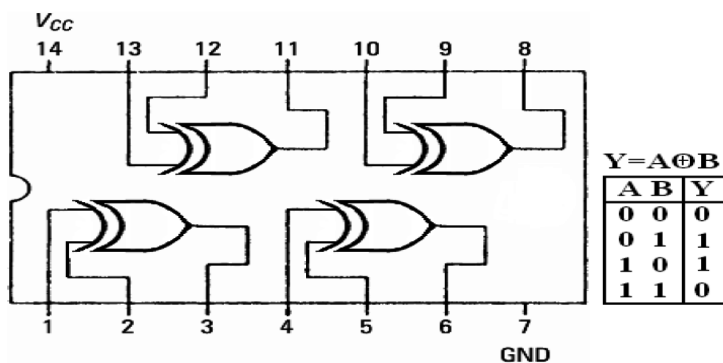


Figure 1.5 EX-OR Gate IC 7486 and truth table

b) Actual Circuit used in laboratory

c) Actual Experimental set up used in laboratory**IX Resources Required**

S. No.	Instrument /Components	Specification	Quantity	Remarks
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	7486, 7404, 7432, 7408	1 Each	
6	LED	Red /Yellow color 5 mm	1	
7	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8	Resistor	1.1 K Ω or 330 Ω	As required	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Identify pin configuration of logic gate IC (7408) and test with digital IC Tester.
2. Make the connections as per figure 1.1 on breadboard and give supply voltage to relevant pin as per logic level.
3. Observe the LED (on or off) for each combination of input as per truth table.
4. Verify the truth table.
5. Repeat the process for IC 7404, 7432, 7486.

XII Resources used (with major specifications)

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual procedure followed (Use blank sheet provided if space not sufficient)

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XIV Precautions followed (Use blank sheet provided if space not sufficient)

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XV Observations and Calculations**Table 1.1: Observation table**

Inputs		7404 (NOT)		7408(AND)		7432(OR)		7486(EX-OR)	
A	B	LED Status (ON/OFF)	Output voltage(v)	LED Status (ON/OFF)	Output voltage	LED Status (ON/OFF)	Output voltage	LED Status (ON/OFF)	Output voltage
0(0V)	0(0V)								
0(0V)	1(5V)								
1(5V)	0(0V)								
1(5V)	1(5V)								

XVI Results

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XVII Interpretation of results (Give meaning of the above obtained results)

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XVIII Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

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XX References / Suggestions for further reading

1. http://www.electronics-tutorials.ws/logic/logic_1.html
2. https://www.youtube.com/watch?v=AT_GjUjNFpo
3. <https://www.youtube.com/watch?v=EBlgoycFNJ8>
4. <https://www.youtube.com/watch?v=LBuLmC0chyQ>
5. <https://www.youtube.com/watch?v=WGYEpZQnRE8>
6. <http://www.ti.com/lit/ds/symlink/sn74ls00.pdf>

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Verification of voltage	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.2: Test the functionality of universal logic gates.

I Practical Significance

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

II Relevant Program Outcomes (POs)

- **Basic knowledge:** Apply knowledge of basic mathematics, sciences and basic engineering to solve the broad-based Electronics and Computer engineering problems
- **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
- **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
- **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency: **‘Build/ test digital logic circuits consist of digital ICs.’**

1. Verify voltage level for logic 0 and 1.
2. Identify pin configuration of logic gate IC’s.
3. Test the functionality of the logic gates.

IV Relevant Course Outcome(s)

- Use Boolean expressions to realize logic circuits.

V Practical Outcome

- Test the functionality of NAND and NOR gate using breadboard (IC 7400 and 7402).

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

OR,AND and NOT gates are the three basic logic gates as they together can be used to construct the logic circuit for any given Boolean expression. NOR and NAND gates have the property that they individually can be used to implement logic circuit corresponding to any given Boolean expression.

The NAND and NOR gates are known as universal gates.

VIII Practical Circuit diagram

a) Sample

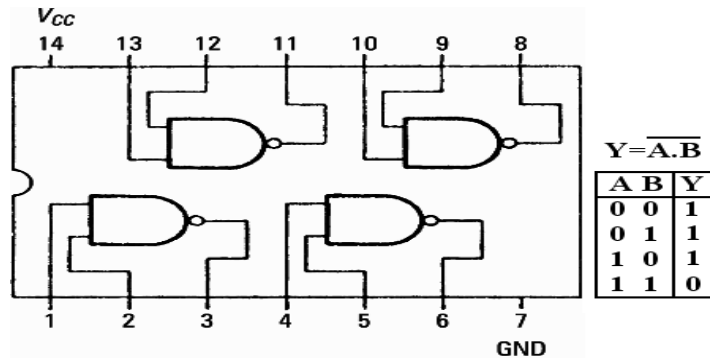


Figure 2.1.NAND Gate IC 7400 and Truth table

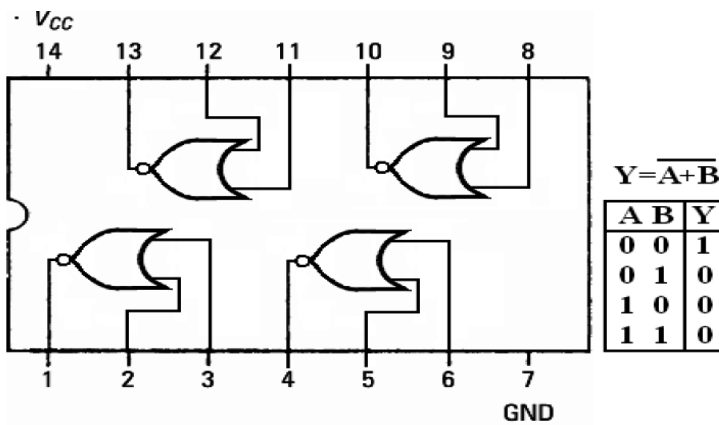


Figure 2.2.NOR Gate IC 7402 and Truth table

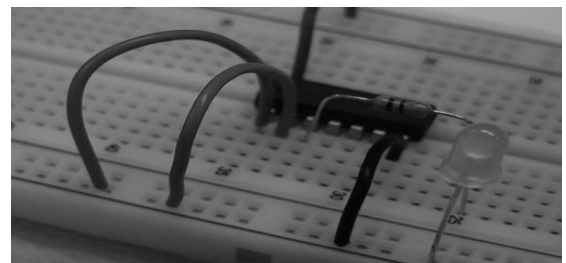
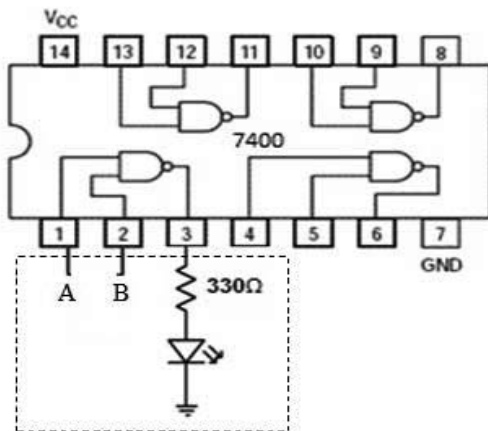


Figure 2.3: Sample Circuit

b) Actual Circuit used in laboratory

c) Actual Experimental set up used in laboratory

IX Resources Required

S. No.	Instrument /Components	Specification	Quantity	Remarks
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2.	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3.	DC power supply	+5 V Fixed power supply	1	
4.	Breadboard	5.5cm X 17 cm	1	
5.	IC	7400, 7402	1 Each	
6.	LED	Red /Yellow color 5 mm	1	
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8.	Resistor	1K Ω or 330 Ω	As required	

X Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Identify pin configuration of logic gate IC (7400) and test with digital IC tester.
2. Make the connections as per figure 2.3 on breadboard and give supply voltage to relevant pin as per logic level.
3. Observe the LED (on or off) for each combination of input as per truth table.
4. Verify the truth table.
5. Repeat the process for IC 7402.

XII Resources used (with major specifications)

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual procedure followed (Use blank sheet provided if space not sufficient)

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XIV Precautions followed (Use blank sheet provided if space not sufficient)

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XV Observations and Calculations.

Table 2.1

Inputs		7400 (NAND)		7402(NOR)	
A	B	LED Status (ON/OFF)	Output voltage	LED Status (ON/OFF)	Output voltage
0(0V)	0(0V)				
0(0V)	1(5V)				
1(5V)	0(0V)				
1(5V)	1(5V)				

XVI Results

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XVII Interpretation of results (Give meaning of the above obtained results)

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XVIII Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

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XIX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. List the function of pin 7 and 14 of IC 7400.
2. Write down name of manufacturer of Digital IC 7400, 7402 used in practical.
3. Suggest another IC used as NAND, AND, NOR Gate.
4. Write the IC no. which has three input NAND & NOR gate.

[Space for answer]

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XX References / Suggestions for further reading

1. www.alldatasheet.com/datasheet-pdf
2. http://www.electronics-tutorials.ws/logic/logic_1.html
3. <https://www.youtube.com/watch?v=nDOCqIVUdk4>
4. <https://www.youtube.com/watch?v=146DbuTCzGQ&t=14s>

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Verification of voltage	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.3: Construct basic gates using universal gates.

I Practical Significance

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

II Relevant Program Outcomes (POs)

- **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
- **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
- **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: **‘Build/ test digital logic circuits consist of digital ICs.’**

- i. Identify pin configuration of logic gate IC’s.
- ii. Verify truth table of logic gates.
- iii. Connect NAND gate and NOR gate IC to implement AND, OR and NOT gates.

IV Relevant Course Outcome(s)

- Use Boolean expressions to realize logic circuits.

V Practical Outcome

- Construct AND, OR, NOT gates using universal gates.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates.

VIII Practical Circuit diagram

a) Sample

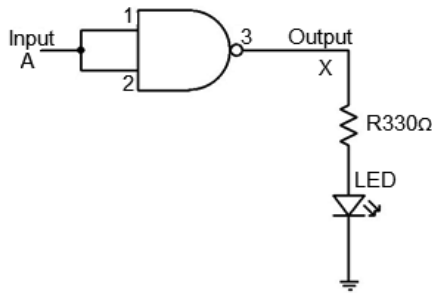


Figure (a)

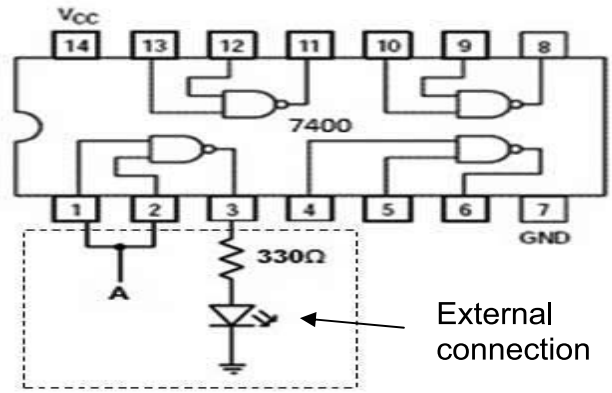


Figure (b)

**Figure 3.1 NOT Gate using NAND a) Logic diagram b) IC Circuit diagram
(Use appropriate value of resistor . Diagram shows sample values)**

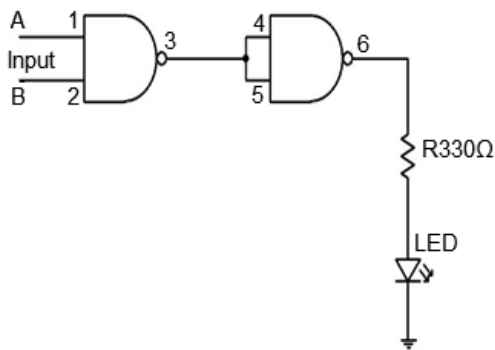


Figure (a)

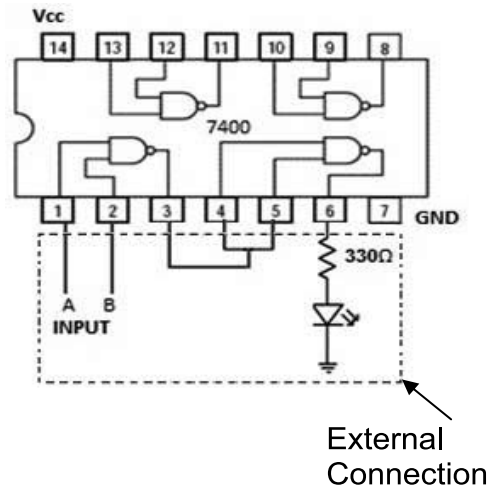


Figure (b)

Figure 3.2 AND Gate using NAND a) Logic diagram b) IC Circuit diagram

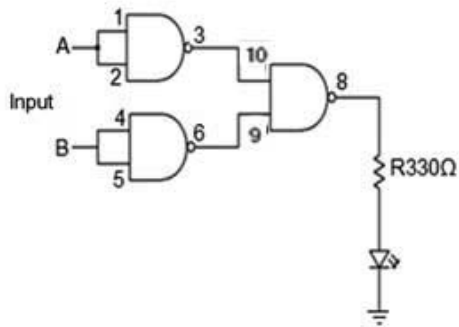


Figure (a)

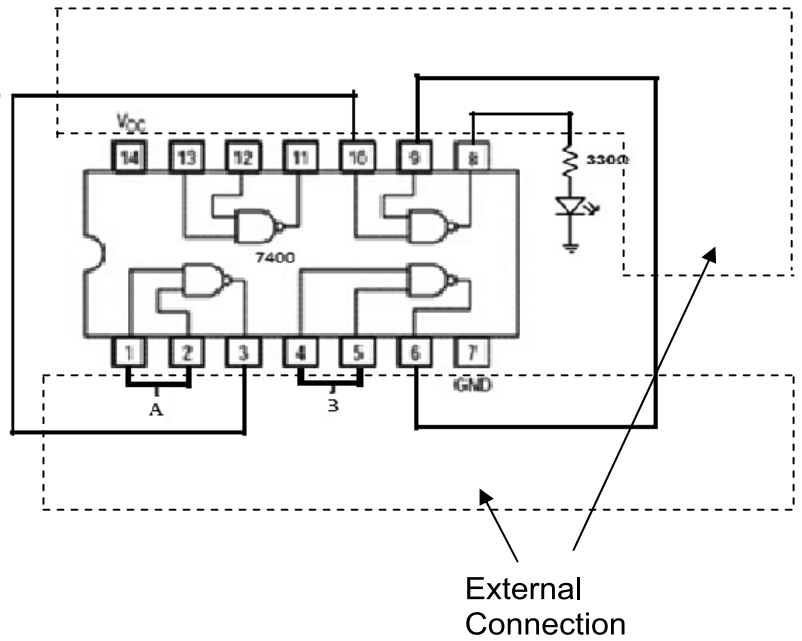


Figure (b)

Figure 3.3 OR Gate using NAND a) Logic diagram b) IC Circuit diagram

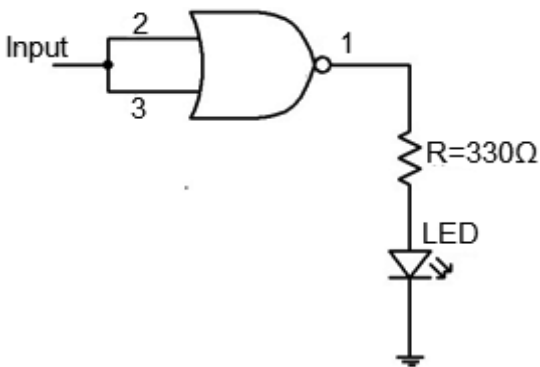


Figure (a)

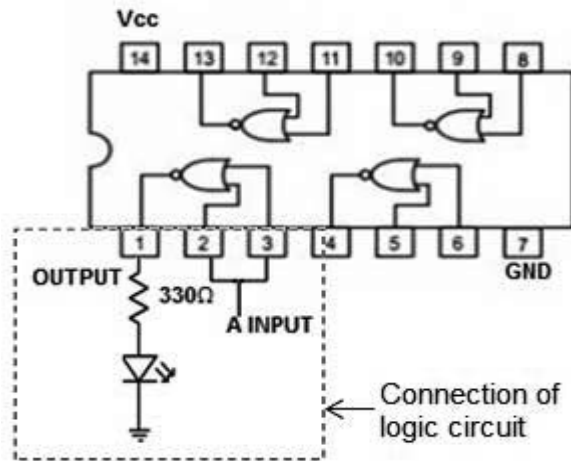


Figure (b)

Figure 3.4. NOT Gate using NOR a) Logic diagram b) IC Circuit diagram

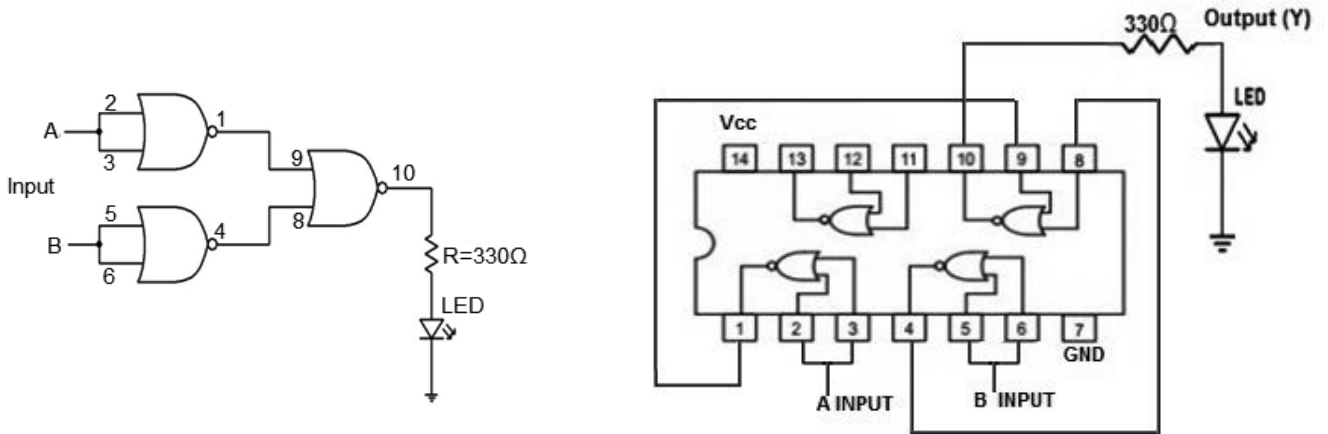
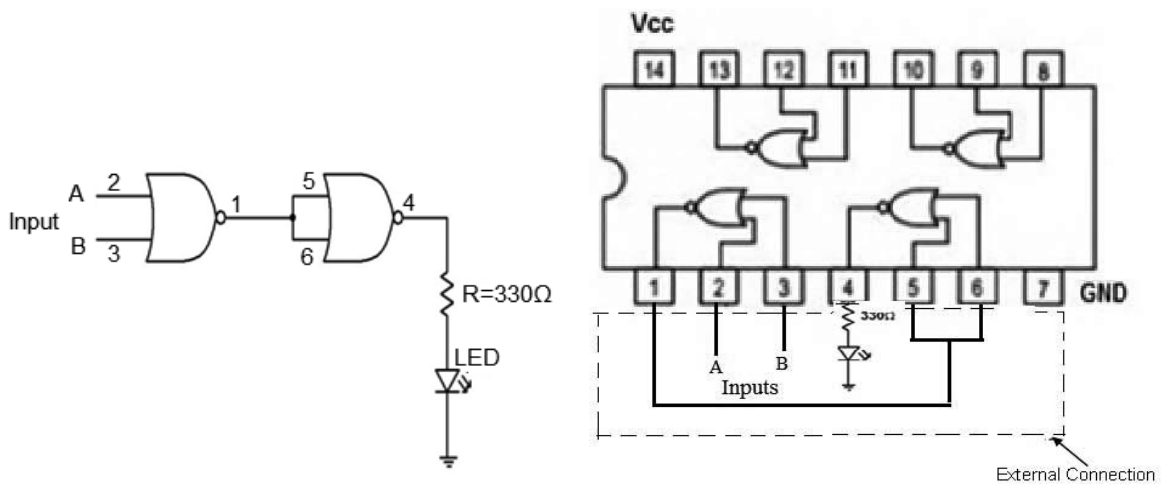


Figure (a) **Figure (b)**
Figure 3.5. AND Gate using NOR a) Logic diagram b) IC Circuit diagram



Figure(a) **Figure (b)**
Figure 3.6. OR Gate using a NOR a) Logic diagram b) IC Circuit diagram

b) Actual Circuit used in laboratory

c) Actual Experimental set up used in laboratory

IX Resources Required

S. No.	Instrument /Components	Specification	Quantity	Remarks
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2.	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3.	DC power supply	+5 V Fixed power supply	1	
4.	Breadboard	5.5cm X 17 cm	1	
5.	IC	7400, 7402	1 Each	
6.	LED	Red /Yellow color 5 mm	1	
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8.	Resistor	1K Ω /330 Ω	As required	

X Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Identify pin configuration of logic gate IC 7400 and test with digital IC Tester.
2. Make the connection as shown in figure 3.1-3.3 on breadboard and give supply voltage to relevant pins per logic level.
3. Observe the LED (on / off) for each combination of input as per truth table.
4. Verify the truth table.
5. Repeat the process for figure 3.4-3.6.

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			

XIII Actual procedure followed (Use blank sheet provided if space not sufficient)

.....

XIV Precautions followed (Use blank sheet provided if space not sufficient)

.....

XV Observations and Calculations

Table 3.1: Observations

Inputs		AND		OR		NOT	
A	B	LED Status (ON/OFF)	Output voltage	LED Status (ON/OFF)	Output voltage	LED Status (ON/OFF)	Output voltage
0(0V)	0(0V)						
0(0V)	1(5V)						
1(5V)	0(0V)						
1(5V)	1(5V)						

XVI Results

.....

XVII Interpretation of results (Give meaning of the above obtained results)

.....

XVIII Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

.....

XX References / Suggestions for further reading

1. <https://www.youtube.com/watch?v=1psl6qRSh4U>
2. <https://www.youtube.com/watch?v=WAXvNfXCcU>

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.4: Verify De Morgan's theorems.

I Practical Significance

Logic gates are the basis units to implement complex logic functions. De Morgan's Theorems are used to simplify the complex Boolean/Logic functions. This practical will enable the students to use De Morgan's theorem to simplify the complex function for the efficient hardware implementation.

II Relevant Program Outcomes (POs)

- **Basic knowledge:** Apply knowledge of basic mathematics, sciences and basic engineering to solve the broad-based Electronics and Computer engineering problems.
- **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
- **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
- **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency: '**Build/ test digital logic circuits using digital ICs.**'

1. Identify pin configuration of IC's.
2. Test the functionality of the logic gates.
3. Apply De Morgan's Theorem to simplify Boolean expressions.

IV Relevant Course Outcome(s)

- Use Boolean expressions to realize logic circuits.

V Practical Outcome

- Build the logic circuit on breadboard to check the De Morgan's theorems.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

De Morgan's theorem is used to simplify Boolean expressions and digital circuits.

De Morgan's first Theorem: It states that for any two elements A and B in a Boolean algebra, the complement of the sum is equal to product of complements.

The theorem can be expressed by logic circuit as

$$\overline{A + B} = \bar{A} \cdot \bar{B}$$

NOR gate = Bubbled AND gate

De Morgan's theorem is used to simplify Boolean expressions and digital circuits.

De Morgan's second Theorem: It states that for any two elements A and B in a Boolean algebra, the complement of a product is equal to the sum of the complements. The theorem can be expressed by logic circuit as

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

NAND gate = Bubbled OR gate

VIII Practical Circuit diagram

a) Sample

De Morgan's first theorem:

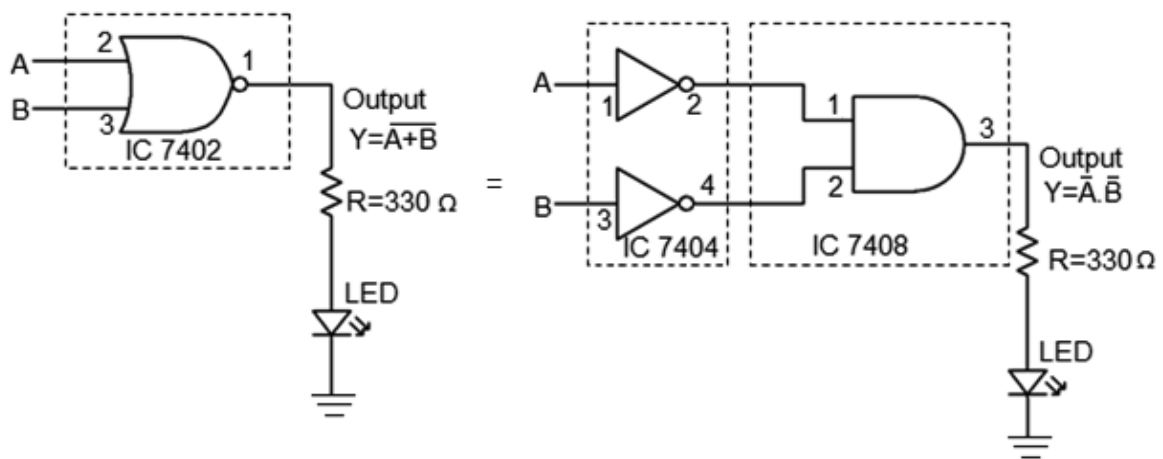


Figure 4.1 De Morgan's first theorem

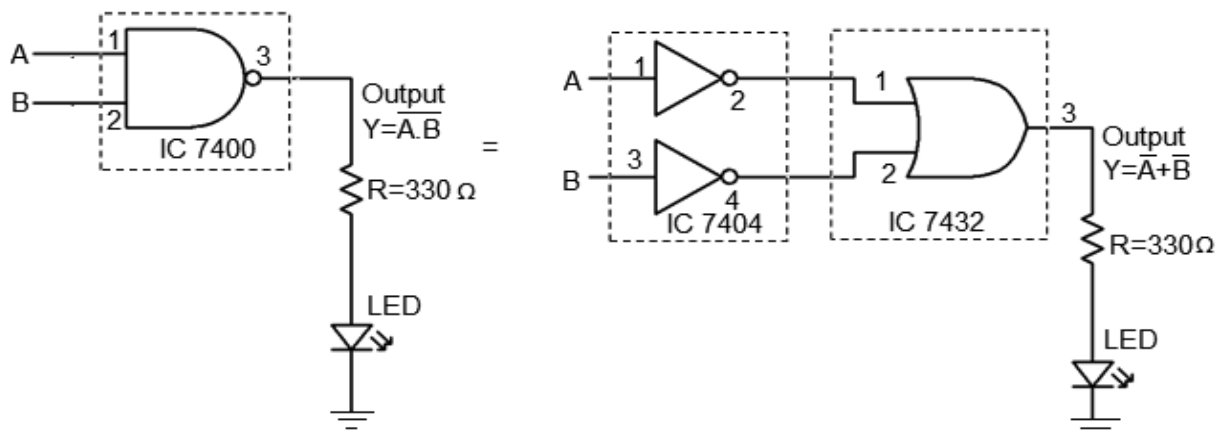


Figure 4.2 De Morgan's second theorem

b) Actual Circuit used in laboratory

c) Actual Experimental set up used in laboratory

IX Resources Required

S. No.	Instrument /Components	Specification	Quantity	Remarks
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2.	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3.	DC power supply	+5 V Fixed power supply	1	
4.	Breadboard	5.5cm X 17 cm	1	
5.	IC	7400, 7404,7432,7402,7208,	1 Each	
6.	LED	Red /Yellow color 5 mm	1	
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	

X Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Identify pin configuration of logic gate IC and test with digital IC Tester.
2. Make the connections as per figure 4.1 on breadboard and give supply voltage to relevant pin as per logic level.
3. Observe the LED (on or off) for each combination of input as per truth table
4. Verify the truth table.
5. Repeat the process for figure 4.2.

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual procedure followed (Use blank sheet provided if space not sufficient)

.....

XIV Precautions followed (Use blank sheet provided if space not sufficient)

.....

XV Observations and Calculations

Table 4.1: De Morgan’s first theorem observation:

Inputs		Outputs	
A	B	LHS= $\overline{A + B}$	RHS= $\overline{A} \cdot \overline{B}$
0	0		
0	1		
1	0		
1	1		

Table 4.2: De Morgan’s second theorem observation:

Inputs		Outputs	
A	B	LHS= $\overline{\overline{A} \cdot \overline{B}}$	RHS= $\overline{\overline{A}} + \overline{\overline{B}}$
0	0		
0	1		
1	0		
1	1		

XVI Results

.....

XVII Interpretation of results (Give meaning of the above obtained results)

.....

XVIII Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

.....

XIX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. List the IC numbers used in De Morgan’s first theorem.
2. List the IC numbers used in De Morgan’s second theorem.
3. Why do we reduce the expression with the help of Boolean algebra and De-Morgan’s theorem?

[Space for answer]

A series of horizontal dotted lines providing space for the student to write their answer.

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XX References / Suggestions for further reading

1. <https://www.youtube.com/watch?v=yueqp943VWE>.

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.5: Design Half adder and half subtractor using boolean expressions.

I Practical Significance:

Digital computers perform variety of information tasks. Among the functions encountered is the various arithmetic operations, the most basic arithmetic operation is the addition or subtraction of two binary digits. A binary adder-subtractor is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers.

II Relevant Program Outcomes (POs)

- **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
- **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
- **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified Competency through various teaching learning experiences: competency: **'Build Combinational logic circuits consist of digital ICs.'**

- i. Testing of IC's on IC tester.
- ii. Identify pin configuration for gates.
- iii. Make connections as per circuit diagram.

IV Relevant Course Outcome(s)

- Build simple combinational circuits.

V Practical Outcome

- Design half adder and half subtractor using Boolean expressions.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

A half-adder is composed of one X-OR gate and one AND gate that produces two binary outputs from two binary inputs. It adds two one-bit binary numbers (A, B). The output is the sum of the two bits (S) and the carry C. The C output is 1 only when both inputs are 1. The S output represents the least significant bit of the sum.

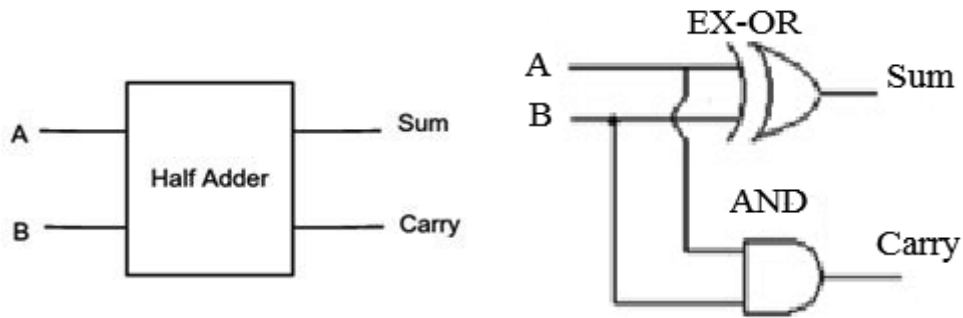


Figure 5.1 Half Adder

A half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, A (minuend) and B (subtrahend) and two outputs D (difference) and B(borrow). It is made of X-OR gate, NOT gate (Inverter), and AND gate. The B output is 1 only when the subtrahend (B) is greater than the minuend (A).

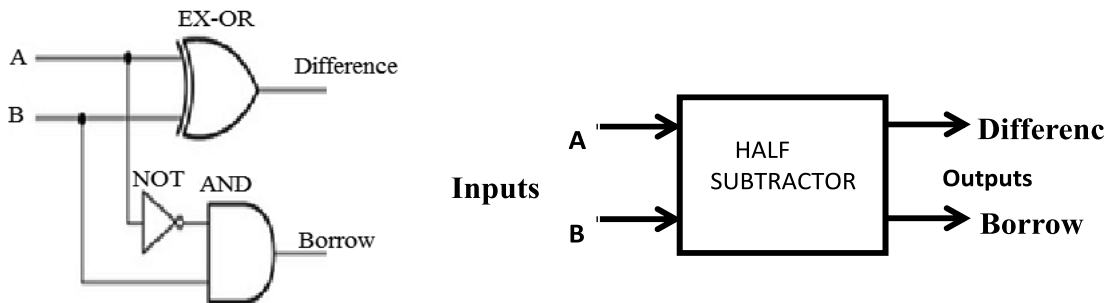


Figure 5.2 Half Subtractor

VIII Practical set-up / Circuit diagram

a) Sample

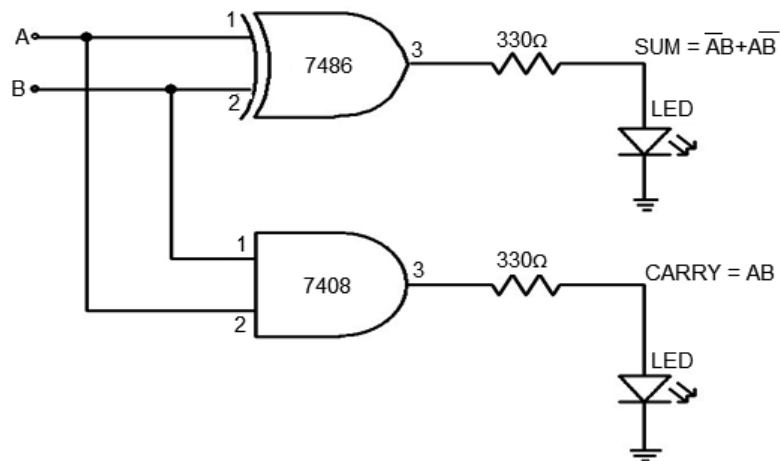


Figure 5.3 Half Adder Circuit

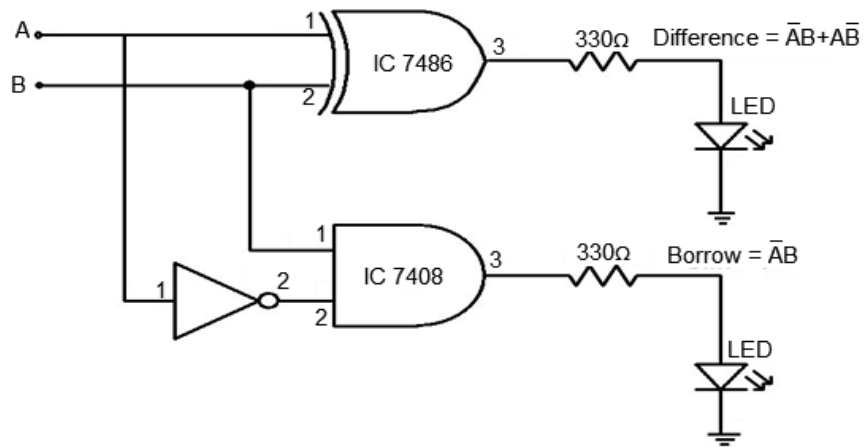


Figure 5.4 Half subtractor Circuit

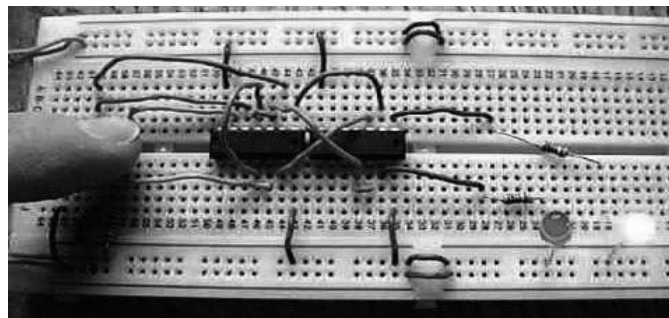


Fig 5.5 Practical Setup

b) Actual circuit used in laboratory

c) Actual Experimental set up used in laboratory

IX Resources Required

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1.	Digital Multimeter	Digital Multimeter:3 ½ digital display	1	
2.	IC Tester	Digital IC Tester	1	
3.	Breadboard	5.5cm X 17 cm	1	
4.	DC power supply	+5 V Fixed power supply	1	
5.	IC 1	7486	1	
6.	IC 2	7404	1	
7.	IC 3	7408	1	
8.	LED	Red /Yellow color 5 mm	2	
9.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
10.	Resistors	330 Ω/0.25 W	2	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Test the IC's using IC tester.
2. Mount IC's on breadboard
3. Set up a half adder and half subtractor circuit and feed all the input combinations
4. Observe the outputs corresponding to input combinations on LEDs.
5. Fill up the observation table.
6. The supply voltage to the IC's should not exceed +5V.

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

.....

XIV Precautions Followed (Use blank sheet provided if space not sufficient)

.....

XV Observations and Calculations:
Observation Table for Half Adder

Input		Output	
A	B	Sum	Carry
0	0		
0	1		
1	0		
1	1		

Observation Table for Half Subtractor

Input		Output	
A	B	Difference	Borrow
0	0		
0	1		
1	0		
1	1		

XVI Results

1.
2.

XVII Interpretation of Results (Give meaning of the above obtained results)

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.....

XVIII Conclusions and Recommendations (Actions/decisions to be taken based on the interpretation of results).

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XIX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

1. Write down drawback of Half Adder circuit.
2. Draw half adder using NAND gates only.
3. Draw Half Subtractor circuit using NAND gates.
4. Design Half Adder/Half Subtractor using K-map.

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[Space for Answers]

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XX References / Suggestions for further reading

1. <https://www.geeksforgeeks.org/half-adder-half-subtractor-using-nand-nor-gates/>
2. <https://www.electronicshub.org/binary-adder-and-subtractor/>
3. www.ahirlabs.com
4. <https://en.wikipedia.org/wiki/Subtractor>

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Test the IC's using IC tester	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.6: Design Full adder and full subtractor.

I Practical Significance:

Digital computers perform variety of information tasks. Among the functions encountered are the various arithmetic operations. The most basic arithmetic operation is the addition or subtraction of binary digits. A binary adder-subtractor is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers. In this practical, students will build circuit and perform addition and subtraction of 3 bits.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: '**Build Combinational logic circuits consist of digital ICs.**'

- i. Testing of IC's on IC tester.
- ii. Identify pin configuration for gates.
- iii. Make connections as per circuit diagram.

IV Relevant Course Outcome(s)

- Build simple combinational circuits.

V Practical Outcome

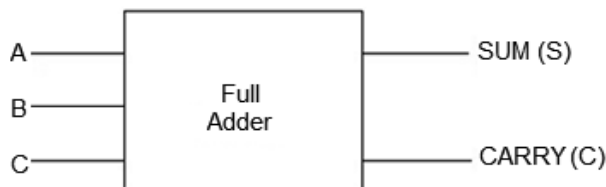
- Design Full adder and full subtractor.

VI Relevant Affective domain related Outcome(s)

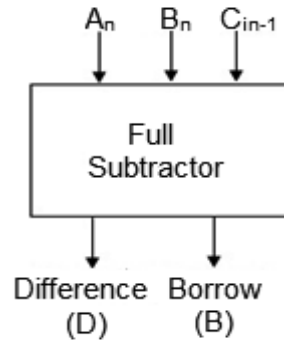
- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

The full adder is a combinational circuit which is used to perform addition of three input bits. Full adder is difficult to implement than a half-adder. The difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry as C-IN and outputs are sum(S) and carry(C).



Full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend. In full subtractor '1' is borrowed by the previous adjacent lower minuend bit. Hence these three bits are considered at the input of a full subtractor. There are two outputs, that are DIFFERENCE output D and BORROW output B.



VIII Practical set-up / Circuit diagram

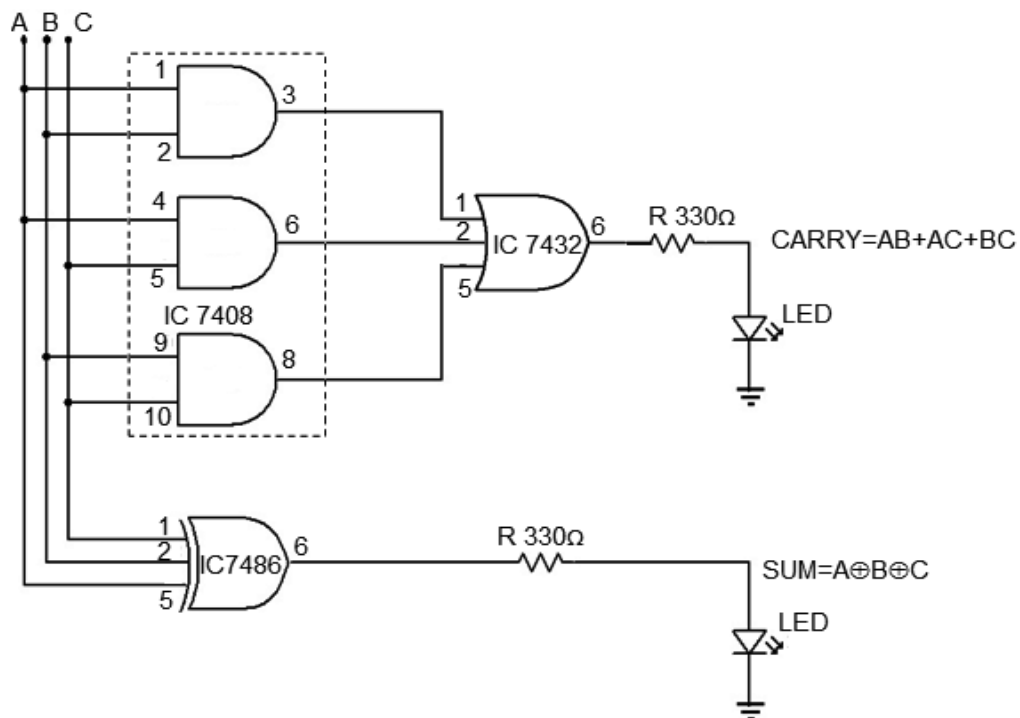


Figure 6.1 Full Adder Circuit

Note : Pin no 3 and pin no 4 of IC 7432 and 7486 are shorted to make 3 input gate

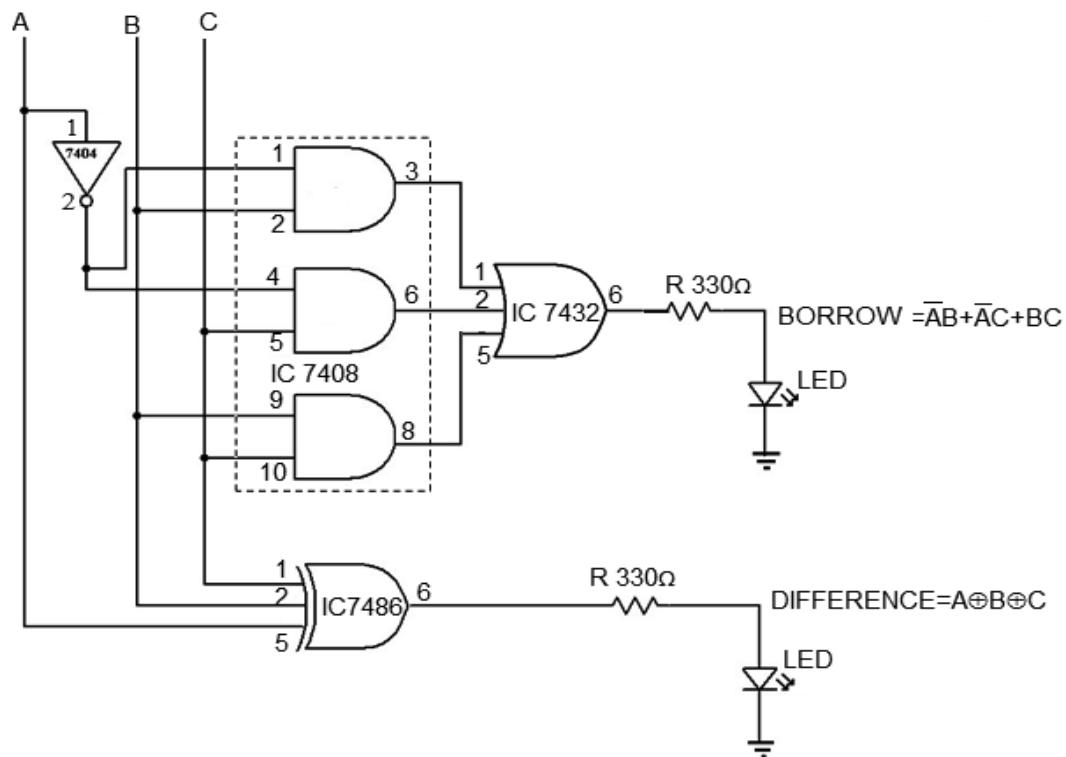


Figure 6.2 : Full Subtractor circuit

Note: Pins 3 and 4 of IC 7432 and 7486 are shared to make 3 input gate

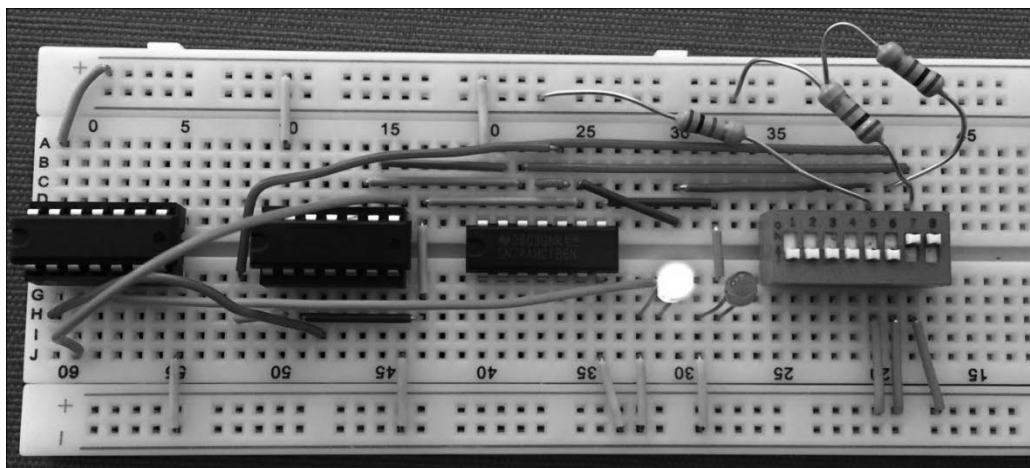


Figure 6.3: Practical Setup

a) Actual circuit used in laboratory

b) Actual Experimental set up used in laboratory

IX Resources Required

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1	Multimeter	Digital Multimeter:3 ½ digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboard	5.5cm X 17 cm	1	
4	DC power supply	+5 V Fixed power supply	1	
5	IC 1	7486	1	
6	IC 2	7404	1	
7	IC 3	7408	1	
8	IC 4	7432	1	
9	LED	Red /Yellow color 5 mm	2	
10	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
11	Resistors	330 Ω,0.25 W	2	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Test the IC's using IC tester.
2. Mount IC's on breadboard.
3. Understand working of all the circuit.
4. Set up full adder and full subtractor circuit and feed all the input combinations
5. Observe the outputs corresponding to input combinations on LEDs.
6. Fill up the observation table.
7. The supply voltage to the IC's should not exceed +5V.

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

1.
2.

XIV Precautions Followed (Use blank sheet provided if space not sufficient)

1.
2.

XV Observations and Calculations:

Observation Table for Full Adder:-

Input			Output	
A	B	C	Sum	Carry
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Observation Table for Full Subtractor:-

Input			Output	
A	B	C	Difference	Borrow
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

XVI Results

1.
2.

XVII Interpretation of Results (Give meaning of the above obtained results)

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XVIII Conclusions and recommendations

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XX References / Suggestions for further reading

1. <https://www.youtube.com/watch?v=RK3P9L2ZXk4>
2. <https://www.youtube.com/watch?v=mZ9VWA4cTbE>
3. <https://www.slideshare.net/JaiminDarji3/design-half-full-adder-and-subtractor>

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Test the IC's using IC tester	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.7: Construct and test BCD to 7 segment decoder using IC 7447/ 7448.

I Practical Significance: BCD is an abbreviation for binary-coded decimal. A Digital Decoder IC, is a device which converts one digital format into another and one of the most commonly used devices for doing this is called the BCD to 7-Segment Display Decoder. It is used to display decimal numbers.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: **'Build Combinational logic circuits consist of digital ICs.'**

- i. Test seven segment display.
- ii. Assemble the circuit on breadboard.
- iii. Make connections as per circuit diagram.

IV Relevant Course Outcome(s):

- Build simple combinational circuits.

V Practical Outcome

- Construct and test BCD to 7 segment decoder using IC 7447/ 7448

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practice

VII Minimum Theoretical Background

A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of 2^n unique output lines. The IC7447 is a BCD to 7-segment pattern converter. The IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs the relevant 7 segment code. A seven segment decoder is an IC decoder that can be used to drive a seven segment indicator. There are two types of 7-segment LED digital display 1. Common anode display (CAD) and 2.Common cathode display (CCD). Each decoder driver has 4 BCD inputs and 7 output pins (a to g segment).

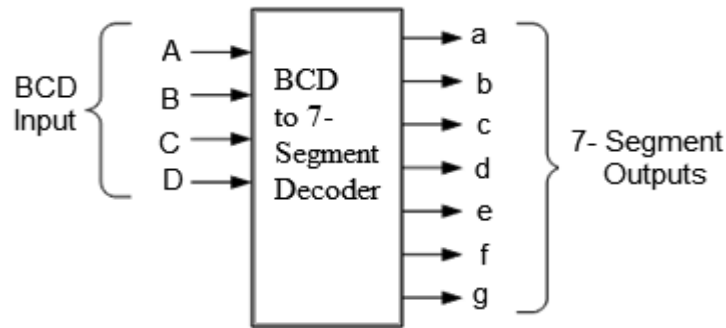


Figure 7.1 BCD to 7-Segment Decoder

Common Cathode Display (CCD):

Common cathode has all the cathodes of the 7-segments connected directly together to ground (Logic 0). The individual segments are illuminated by application of high (Logic 1) signal to the individual anode terminals. For common cathode LED display the ICs are IC 7448, IC 74248, IC 7449 etc. are used. They have active high, open collector outputs.

Common Cathode Display (CCD):

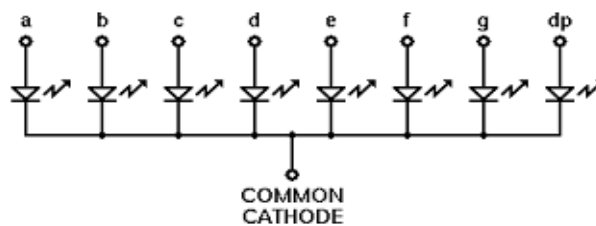


Figure 7.2 Common Cathode Display

Common Anode Display (CAD):

Common anode has all the anodes of the 7-segments connected together to VCC (Logic 1). The individual segments are illuminated by connecting the individual cathode terminals to low (Logic 0) signal to the individual anode terminals. For common anode LED display the ICs are IC 7446, IC 74246, IC 7447 etc. are used. They have active low, open collector outputs.

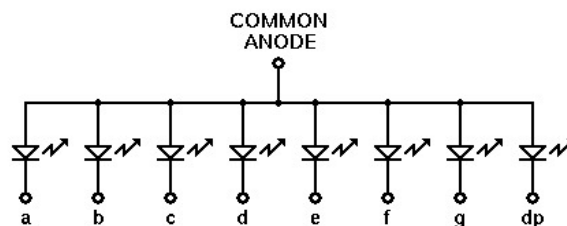


Figure 7.3 Common Anode Display

Courtesy: (<https://arduino.stackexchange.com/questions/16858/leds-difference-between-common-anode-and-common-cathode>)

IC 7447(BCD to 7-Segment decoder IC):-

IC 7447 is BCD to 7-Segment decoder IC whose output is active low depending on the corresponding BCD inputs so it is used to drive common anode 7- segment displays.

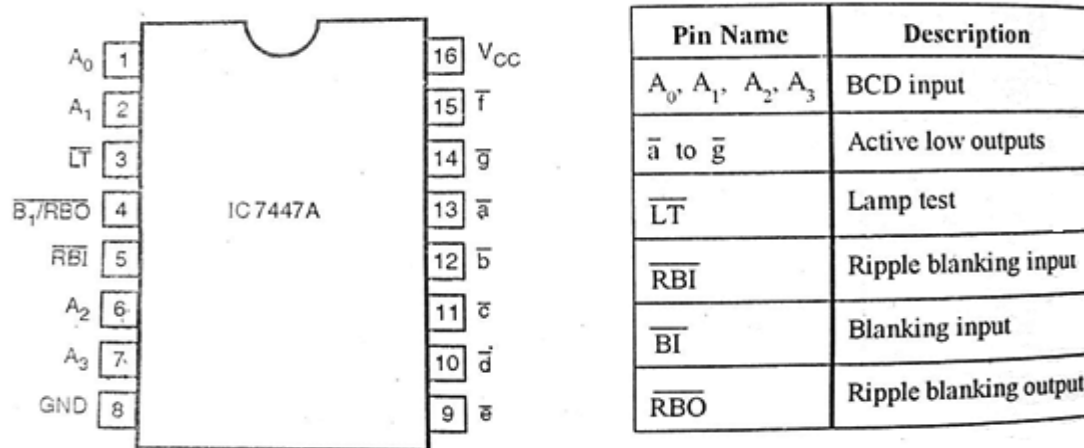


Figure 7.4 IC 7447 Pin Configuration

IC 7448(BCD to 7-Segment decoder IC):-

IC 7448 is BCD to 7-Segment decoder IC whose output is active high depending on the corresponding BCD inputs so it is used to drive common cathode 7- segment displays

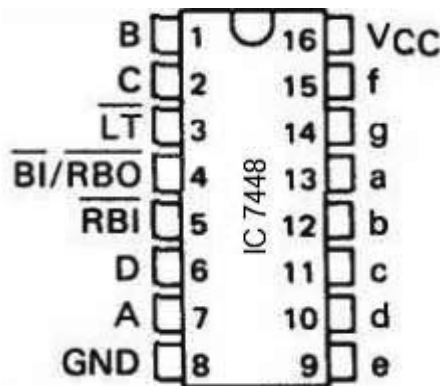
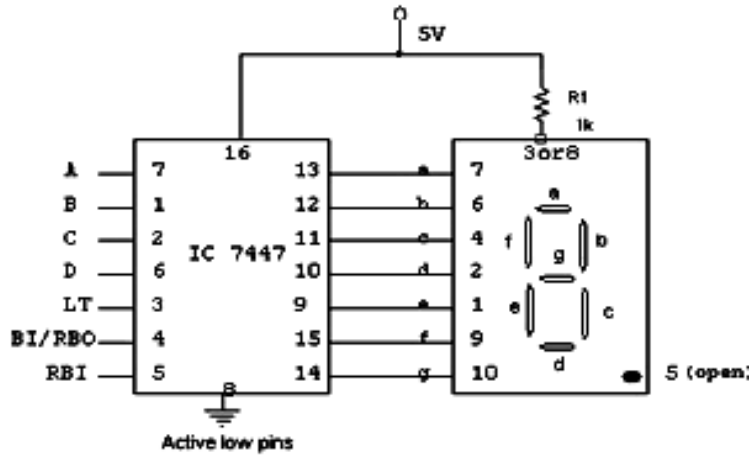


Figure 7.5 IC 7448 Configuration

VIII Practical set-up / Circuit diagram

a) Sample



For normal functioning of IC 7447 Pin number 3, 4, 5 should be connected to logic 1 $\cong V_{cc}$

Courtesy: (<http://www.bragitoff.com/2015/10/bcd-to-7-segment-decoderdriver/>)

Figure 7.6: Circuit diagram

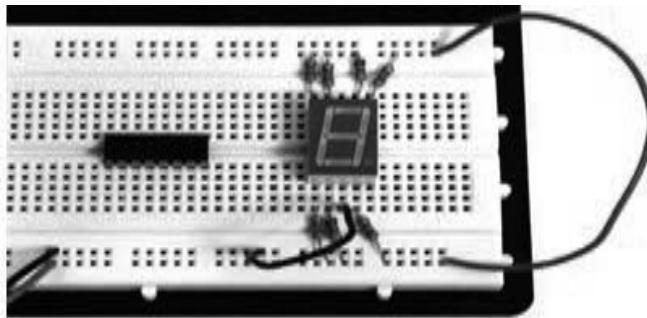


Figure 7.7 : Practical Setup

b) Actual circuit used in laboratory

c) Actual Experimental set up used in laboratory

IX Resources Required

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1.	Digital Multimeter	Digital Multimeter:3 ½ digital display	1	
2.	IC Tester	Digital IC Tester	1	
3.	Breadboard	5.5cm X 17 cm	1	
4.	DC power supply	+5 V Fixed power supply	1	
5.	IC 1	7447	1	
6.	IC 2	7448	1	
7.	Common anode 7-seg Display	IC FND 507/LT 542	1	
8.	Common cathode 7-seg Display	IC LT 543	1	
9.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
10.	Resistors	330 Ω/0.25 W	7	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Test the IC's using IC tester.
2. Mount IC's on breadboard
3. Connect different BCD inputs from 0000 to 1001 and note down the corresponding output on the display.
4. Observe the outputs on 7- segment display.
5. Fill up the observation table.
6. The supply voltage to the IC's should not exceed +5V.

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			



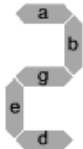
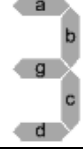

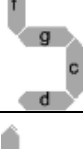
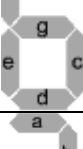
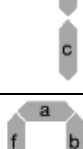

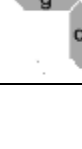
XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

1.
2.

XIV Precautions Followed (Use blank sheet provided if space not sufficient)

1.
2.

XV Observations and Calculations:
Observation Table for Half Adder

BCD inputs				7-SEGMENT CODED OUTPUTS							Display output
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								

BCD Inputs				7-Segment Coded Output						
D	C	B	A	a	b	c	d	e	f	g
0	0	0	0							
0	0	0	1							
0	0	1	0							
0	0	1	1							
0	1	0	0							
0	1	0	1							
0	1	1	0							
0	1	1	1							
1	0	0	0							
1	0	0	1							

XVI Results

1.
2.

XVII Interpretation of Results (Give meaning of the above obtained results)

.....

XVIII Conclusions and recommendations (Actions/decisions to be taken based on the interpretation of results).

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XIX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. Verify and write down the output for 7-segment decoder using common cathode display Practically in table.
2. Write down functions of decoder.
3. Write the functions of pin No. 3, 4, and 5 of IC 7447.
4. List different types of decoder.

[Space for Answers]

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XX References / Suggestions for further reading

1. <https://www.electronics-tutorials.ws/blog/7-segment-display-tutorial.html>
2. https://www.electronics-tutorials.ws/combination/comb_6.html
3. https://en.wikipedia.org/wiki/Seven-segment_display

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Test the IC's using IC tester	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.8: Verify operation of Multiplexer (MUX)

I Practical Significance

In most of the electronic systems, the digital data is available on more than one line. It is necessary to route this data over a single line. Under such circumstances we require a circuit which selects one of the many inputs at a time. This circuit is a multiplexer, which has many inputs, one output and some select inputs. Multiplexer improves the reliability of the digital system because it reduces the number of external wired connections.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.
4. **Individual and team work:** Function effectively as a leader and team member in diverse/ multidisciplinary teams.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency: '**Build/ test digital logic circuits using digital ICs.**'

- i. Identify pin configuration of Multiplexer IC's.
- ii. Test the functionality of the Multiplexer.

IV Relevant Course Outcome(s)

- Build simple combinational circuits.

V Practical Outcome

- Build / test function of MUX 74151/74150 or any other equivalent.
(IC 74151/74150)

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

Multiplexer is a combinational circuit that is one of the most widely used in digital design. The multiplexer is a data selector which gets one out of several inputs to a single output. It has n data inputs and one output line and m select lines where $2^m = n$ shown in figure 8.1. Depending upon the digital code applied at the select inputs one out of n data input is selected and transmitted to a single output channel. Normally strobe (G) input is incorporated which is generally active low which enables the multiplexer when it is LOW. Strobe input helps in cascading. IC 74151A is an 8: 1 multiplexer which provides two complementary outputs Y and \bar{Y} The output Y is same as the selected input and \bar{Y} is its complement. The n : 1 multiplexer can be used to realize m variable function. ($2^m = n$, m is no. of select inputs)

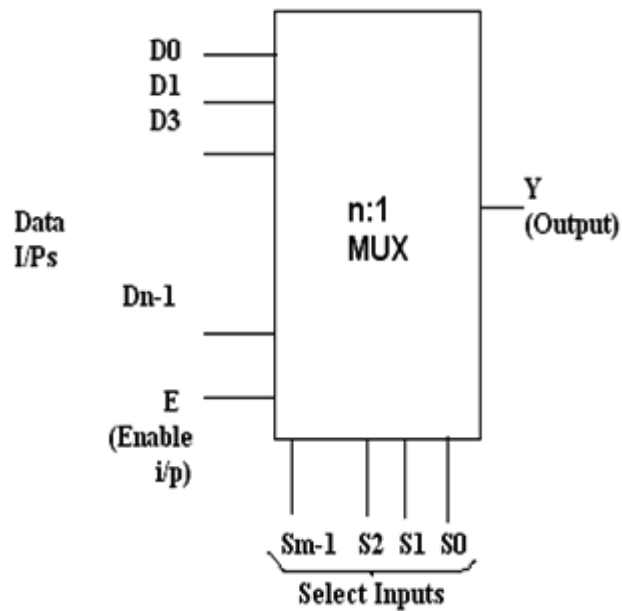


Figure 8.1 Block diagram of n: 1 Multiplexer

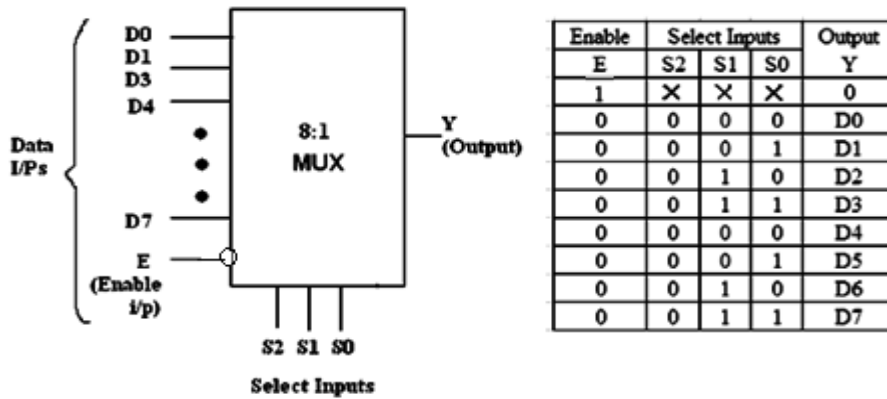
Courtesy: <https://www.google.co.in/search?client=firefox-b&biw=1366&bih=654&tbm=isc>

Types of Multiplexer (MUX):

1. 2:1 MUX (2 lines to 1 line)
2. 4:1 MUX (4 lines to 1 line)
3. 8:1 MUX (8 lines to 1 line)
4. 16:1 MUX (16 lines to 1 line)

List of ICs which provide multiplexing

IC No.	Function	Output State
74157	Quad 2:1 MUX.	Output same as input given
74158	Quad 2:1 MUX.	Output is inverted input
74153	Dual 4:1 MUX	Output same as input
74352	Dual 4:1 MUX	Output is inverted input
74151A	8:1 MUX	Both outputs available (i.e., complementary outputs)
74151	8:1 MUX	Output is inverted input
74150	16:1 MUX	Output is inverted input



(E=1 for active high E=0 for active low)

Figure 8.2: Block diagram of 8: 1 MUX, Truth Table of 8:1 MUX

VIII Practical Circuit diagram

a) Sample

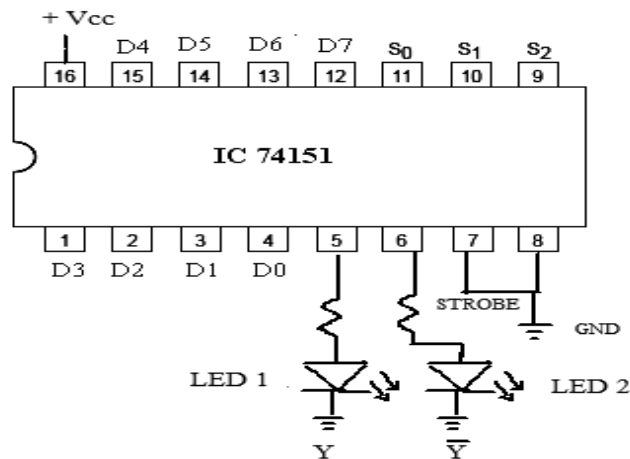


Figure 8.3: Circuit Diagram

b) Actual Circuit used in laboratory

c) Actual Experimental set up used in laboratory**IX Resources Required**

S. No.	Instrument /Components	Specification	Quantity	Remarks
1	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	74151/74150	1	
6	LED	Red /Yellow color 5 mm	1	
7	Resistor	330 Ω	2	
8	Connecting wires	Single strand 0.6 mm Teflon coating	As required	

X Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Test the IC using Digital IC Tester.
2. Mount the IC on the breadboard.
3. Make the connections as per figure 8.3
4. Give the supply voltage to IC +5V.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

XII Resources used (with major specifications)

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual procedure followed (Use blank sheet provided if space not sufficient)

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XIV Precautions followed (Use blank sheet provided if space not sufficient)

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XV Observations and Calculations

Table 8.1: Observation table

Inputs					Outputs	
Strobe	Data input	Select Input			Y	\bar{Y}
G	D _n	S ₂	S ₁	S ₀		
0		0	0	0		
0		0	0	1		
0		0	1	0		
0		0	1	1		
0		1	0	0		
0		1	0	1		
0		1	1	0		
0		1	1	1		
1		X	X	X		

(Write the observation with respective to number of inputs)

(Note: 'X'-indicates the don't care conditions. It means status of select input may be any combination.)

XVI Results

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XX References / Suggestions for further reading

1. <https://www.youtube.com/watch?v=x8N4XI452jM>
2. <https://razorjr.files.wordpress.com/2013/07/multiplexersdemultiplexers.ppt>
3. pesona.mmu.edu.my/.../Week_7_and_8_-_Lecture_3_of_3_-_Multiplexers_and_Dem

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.9: Functionality of Demultiplexer (DEMUX)

I Practical Significance

A demultiplexer (or demux) is a device taking a single input signal and selecting one of many data-output-lines, which is connected to the single input. An electronic demultiplexer can be considered as a single-input, multiple-output switch. Demultiplexers are mainly used in Boolean function generators and decoder circuits.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency: ‘**Build/ test digital logic circuits using digital ICs.**’

- i. Identify pin configuration of IC.
- ii. Test the functionality of the Demultiplexer.

IV Relevant Course Outcome(s)

- Build simple combinational circuits.

V Practical Outcome

- Build / test function of DEMUX 74154/74155 or any other equivalent.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

Demultiplexer has only one input and “n” number of outputs along with “m” number of select inputs. A demultiplexer performs the reverse operation of multiplexer i.e. it receives one input and distributes it over several outputs. At a time only one output line is selected by the select lines and the input is transmitted to the selected output line. Hence demultiplexer is equivalent to a single pole multiple way switch as shown in figure. The enable input will enable the demultiplexer. The relation between the n output lines and m select lines is as given below.

$$n = 2^m$$

The demultiplexer performs opposite process to a multiplexing process it performs “one to many” operation. It has only one input (D) and n number of outputs (Y₀, Y₁, Y₂... Y_{n-1}) as shown in the figure given below. Demultiplexer can also be used as a decoder e.g. Binary to Decimal Decoder. Data input given is I, strobe/enable pin is used for enabling DEMUX

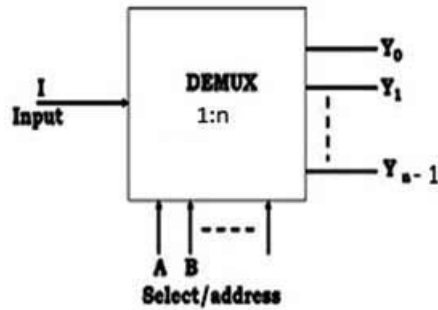


Figure 9.1 Block diagram of 1:nDemultiplexer
 Courtesy:<https://www.electronicshub.org/demultiplexerdemux/13.3.2018>

Types of Demultiplexer (DEMUX):

1. 1:2 DEMUX(1 line to 2 lines)
2. 1:4 DEMUX(1 line to 4 lines)
3. 1:8 DEMUX (1 line to 8 lines)
4. 1:16 DEMUX (1 lines to 16 lines)

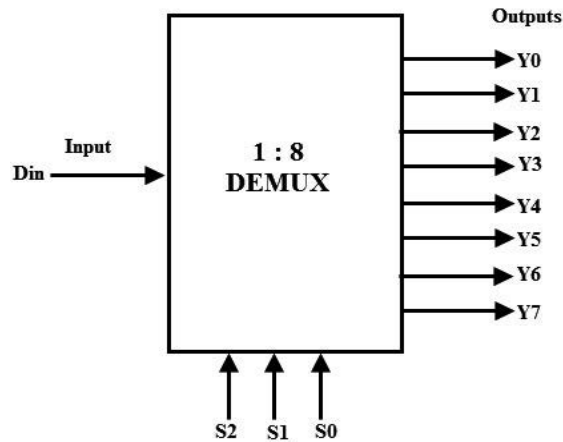


Figure 9.2 Block diagram of 1:8 DEMUX
 Courtesy:<https://www.electronicshub.org/demultiplexerdemux/13.3.2018>

Table 9.1 Truth Table of 1:8 DEMUX

Data Input	Select Inputs			Outputs								
	Din	S ₂	S ₁	S ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
D	0	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	0	D	0	0	0	0	0
D	1	1	0	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0	0

VIII Practical Circuit diagram

a) Sample

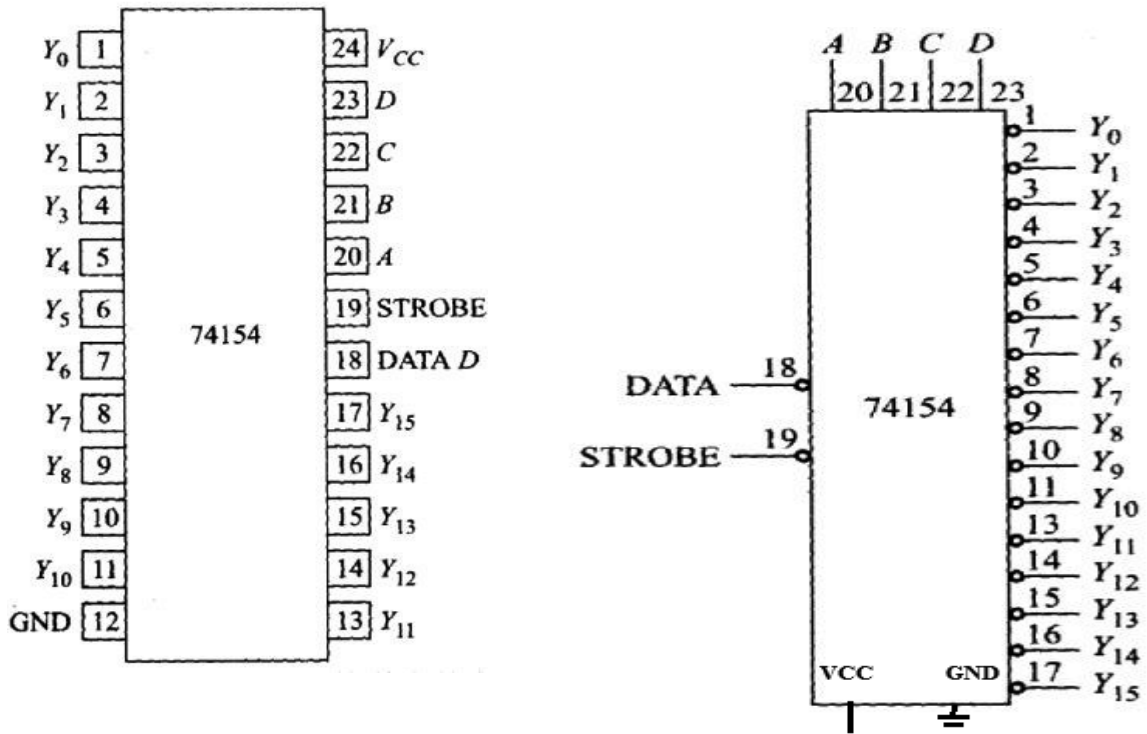


Figure 9.3 Sample circuit Diagram

b) Actual Circuit used in laboratory

c) Actual Experimental set up used in laboratory**IX Resources Required**

S. No.	Instrument /Components	Specification	Quantity	Remark
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2.	Breadboard	5.5cm X 17 cm	1	
3.	DC power supply	+5 V Fixed power supply	1	
4.	IC	74154/74155	Any one	
5.	LED	Red / Yellow color 5 mm	1	
6.	Resistor	330 Ω	4	
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	

X Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Test the IC using Digital IC Tester.
2. Mount the IC on the breadboard.
3. Make the connections as shown in figure 9.3
4. Give the supply voltage to IC +5V.
5. Apply input to select lines according to the observation table.
6. Observe the LED (on or off) for each combination of input as per truth table.
7. Verify the truth table.

XII Resources Used (with major specifications)

S. No.	Instrument /Components	Specification	Quantity	Remark
1.				
2.				
3.				
4.				

XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

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XIV Precautions Followed (Use blank sheet provided if space not sufficient)

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XV Observations and Calculations

Table 1: Observations

Inputs						Outputs																
D _{in}	G	S ₃	S ₂	S ₁	S ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉	Y ₁₀	Y ₁₁	Y ₁₂	Y ₁₃	Y ₁₄	Y ₁₅	
0	0	0	0	0	0																	
0	0	0	0	0	1																	
0	0	0	0	1	0																	
0	0	0	0	1	1																	
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0	1	1	1	1	0																	
0	1	1	1	1	1																	
1	X	X	X	X	X																	

(Note: ‘X’-indicates the don’t care conditions. It means status of select input may be any combination.)

XVI Results

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XVII Interpretation of results (Give meaning of the above obtained results)

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XVIII Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

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XIX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

1. List the function of pin 2, 3 and 5 of IC 74155.
2. List the name of manufacturers of Digital IC used in practical.
3. What is the role of select lines in a Demultiplexer?
4. What is the output of IC 74155 if D0=1, G=1, S3, S2, S1=XXX?
5.

[Space for Answers]

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XX References / Suggestions for further reading

- 1 <https://www.youtube.com/watch?v=x8N4XI452jM>
- 2 <https://razorjr.files.wordpress.com/2013/07/multiplexersdemultiplexers.ppt>
- 3 pesona.mmu.edu.my/.../Week_7_and_8_-_Lecture_3_of_3_-_Multiplexers_and_Dem...

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No. 10: Test functionality of RS flip flop using NAND Gates.

I Practical Significance

A flip-flop is a circuit that has two stable states and can be used to store information. A flip flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or many control inputs and will have one or two outputs. The flip flop is a one bit memory cell it stores one bit of information. The data available in memory can be used for further operation. The flip flops are used in bounce elimination switch, shift registers, counters and in random access memory.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency: ‘**Build/ test digital logic circuits using digital ICs.**’

- i. Identify pin configuration of IC.
- ii. Test the functionality of the RS flip flop.

IV Relevant Course Outcome(s)

- Build simple sequential circuits.

V Practical Outcome

Build / test function of RS flip flop using NAND Gates.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

Digital circuits have many combinations of logic circuits. They are classified as either combinational or sequential. The output of combinational circuits depends only on the current inputs. In contrast, sequential circuit depends not only on the current value of the input but also upon the internal state of the circuit. Basic building blocks (memory elements) of a sequential circuit are the flip-flops (FFs). The FFs change their output state depending upon inputs at certain interval of time synchronized with some clock pulse applied to it.

Types of flip flops

1. SR-FF (Set Reset flip flop)
2. JK-FF (JK flip flop)
3. MSJK-FF(Master Slave JK flip flop)
4. D-FF (Delay flip flop)
5. TFF (Toggle flip flop)

Practical Circuit diagram:-

a) Sample

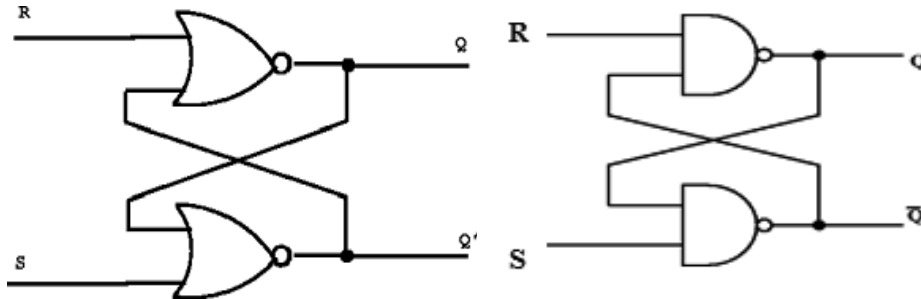


Figure 10.1 a) RS Latch Using NOR

(b) RS Latch Using NAND

S	R	Q	\overline{Q}
0	0	Same as previous	Same as previous
0	1	0	1
1	0	1	0
1	1	Race	Race

S	R	Q	\overline{Q}
0	0	Race	Race
0	1	0	1
1	0	1	0
1	1	Same as previous	Same as previous

Figure 10.2 Truth Table of logic diagram for figure 10.1a, b

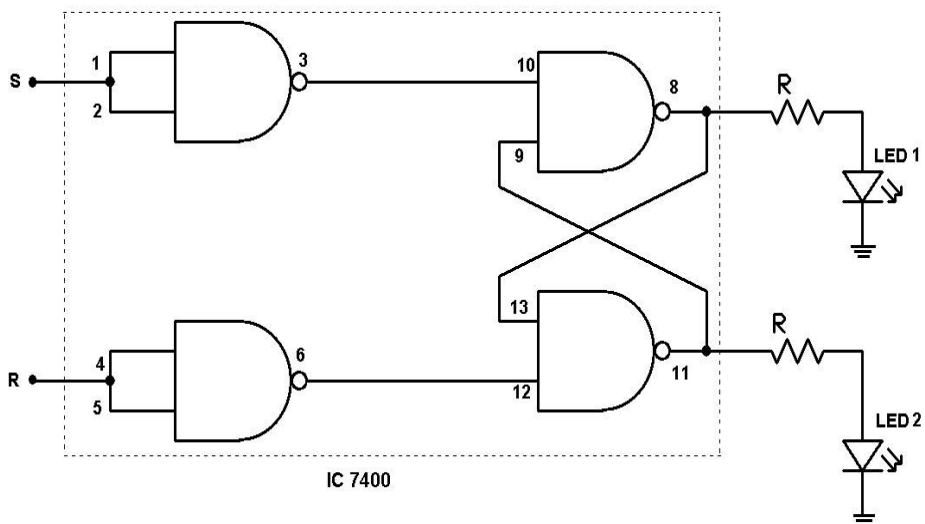


Figure 10.3 RS-FF Using NAND Gate

b) Actual Circuit used in laboratory**c) Experimental setup used in laboratory****VIII Resources Required**

S. No.	Instrument /Components	Specification	Quantity	Remarks
1	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	7400	1 Each	
6	LED	Red /Yellow color 5 mm	2	
7	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8	Resistors	330 Ω	2	

IX Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

X Procedure

1. Mount the IC7400 on the breadboard.
2. Make the connections as shown in figure 10.3
3. Apply the supply voltage to IC +5V.
4. Apply inputs according to the observation table.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

XI Resources used (with major specifications)

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XII Actual procedure followed (Use blank sheet provided if space not sufficient)

.....

XIII Precautions followed (Use blank sheet provided if space not sufficient)

.....

XIV Observations and Calculations

Table 1: Truth Table SR flip-flop

S	R	Q	\overline{Q}	Comment
0	0			
0	1			
1	0			
1	1			

XV Results

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XVI Interpretation of results (Give meaning of the above obtained results)

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XVII Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

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XVIII Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

1. List the name of manufacturer of Digital IC used in practical.
2. Test the output when S=R=1.
3. Test the output when CLK =1, verify truth table. (for clocked input circuit)
4. Test the output when CLK =0, verify truth table (For clocked input circuit)

[Space for answer]

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XX References / Suggestions for further reading

1. www.alldatasheet.com/datasheet-pdf
2. <http://www.electronics-tutorials.ws>
3. <https://academo.org/demos/logic-gate-simulator>

XXI Suggested Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No. 11: Test functionality of MS JK flip flop

I Practical Significance

The limitation of SR flip flop is over come in JK flip flop. In JK flip flop when $J=K=1$, the output is uncertain; this situation is called Race around condition. To avoid the problem of race around condition the JK flip flop in Master and slave mode is used.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer engineering knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: **'Build/ test digital logic circuits using digital ICs.'**

- i. Identify pin configuration of digital IC.
- ii. Test the functionality of the MSJK flip flop.

IV Relevant Course Outcome(s)

- Build simple sequential circuits.

V Practical Outcome

- Build / test function of MS JK flip flop using 7476.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

Master Slave J K flip flop is a cascade of two S-R flip-flops, with feedback from the outputs of the second flip flop to the inputs of the first. The first part is called as master flip-flop while the next is called as slave flip-flop .Here the master flip-flop is triggered by the external clock pulse while the slave is activated at its inversion i.e. if the master is positive level triggered, then the slave is negative-level triggered and vice-versa. This means that the data enters into the flip-flop at positive/negative level of the clock pulse while it is obtained at the output pins during positive/negative level of the clock pulse. Hence a master-slave flip-flop completes its operation only after the appearance of one full clock pulse.

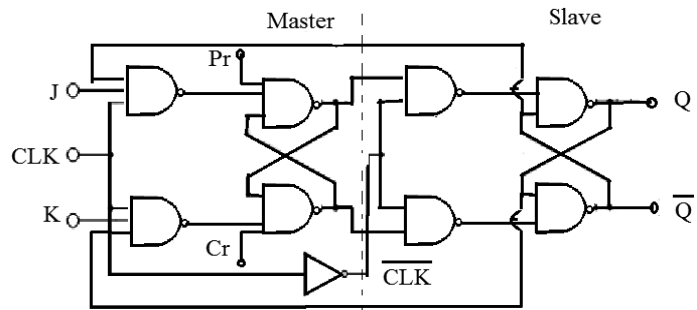


Figure 11.1 Master Slave J-K flip flop

VIII Practical Circuit diagram

a) Sample

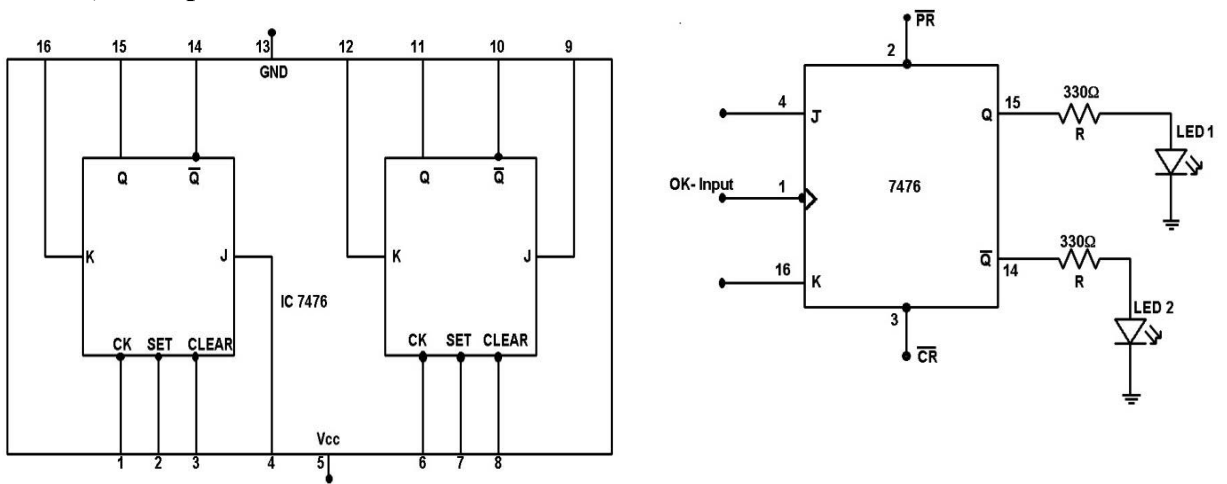


Figure 11.2 a) Pin configuration 7476 b) MS JK FF

Inputs		Output
J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Table 11.1 Truth table of Master Slave JK flip flop

b) Actual Circuit used in laboratory**c) Experimental setup used in laboratory****IX Resources Required**

S. No.	Instrument /Components	Specification	Quantity	Remarks
1	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	7476	1 Each	
6	LED	Red /Yellow color 5 mm	1	
7	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8	Resistor	330 Ω	1	

X Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Mount the IC7476 on the breadboard.
2. Make the connections as shown in figure 11.2b
3. Apply the supply voltage to IC +5V.
4. Apply inputs according to the observation table.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

XII Resources used (with major specifications)

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual procedure followed (Use blank sheet provided if space not sufficient)

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XIV Precautions followed (Use blank sheet provided if space not sufficient)

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XV Observations and Calculations:

Table 2: Truth Table MSJK flip-flop

J	K	Q	\bar{Q}	Comment
0	0			
0	1			
1	0			
	1			

XVI Results

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XX References / Suggestions for further reading

1. www.alldatasheet.com/datasheet-pdf
2. <http://www.electronics-tutorials.ws>
3. <https://academo.org/demos/logic-gate-simulator>

XXI Suggested Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No. 12: Test functionality of D and T flip flop

I Practical Significance

D Flip –Flop (Delay Flip –Flop) is used to provide time delay. They are basic building blocks of Shift Registers T Flip-Flop (Toggle Flip-Flop) experiences a change in output in each clock edge. Hence it can be used as a frequency divider. T Flip-Flop can also be used to design Counters.

II Relevant Program Outcomes (POs)

- **Discipline knowledge:** Apply Electronics and Computer engineering knowledge to solve broad-based Electronics and Computer engineering related problems.
- **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
- **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: **‘Build/ test digital logic circuits using digital ICs.’**

- i. Identify pin configuration of IC.
- ii. Test the functionality of D and T flip flop.

IV Relevant Course Outcome(s)

- Build simple sequential circuits.

V Practical Outcome

- Use IC7476 to construct and test the functionality of D and T flip flop.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background

The D flip-flop is obtained from the JK/SR flip-flop by connecting a NOT gate between the J/S and K/R inputs of the JK/SR flip-flop and T flip-flop is obtained from JK flip-flop by shorting J and K inputs of the JK flip-flop.

VIII Practical Circuit diagram

a) Sample

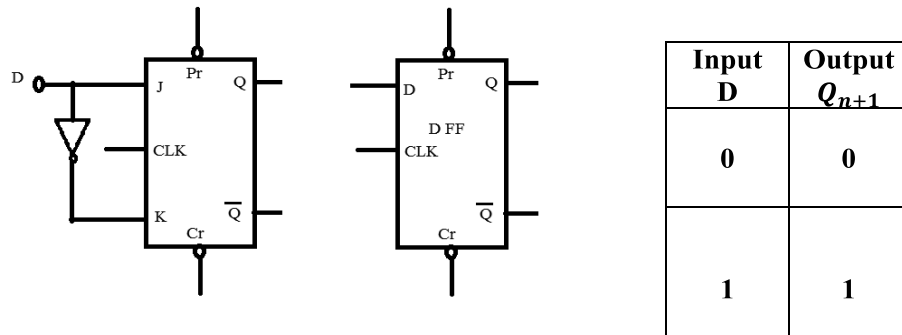


Figure 12.1a) D FF using 7476 b) Symbol c) Truth Table

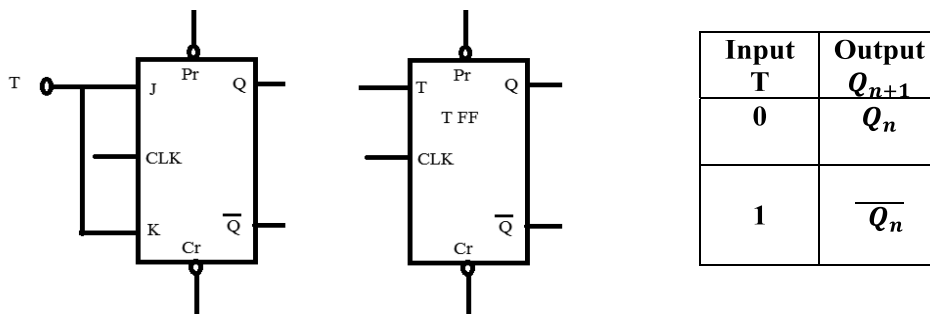


Figure 12.2a) T FF using 7476 b) Symbol c) Truth Table

IX Practical Circuit diagram

a) Sample

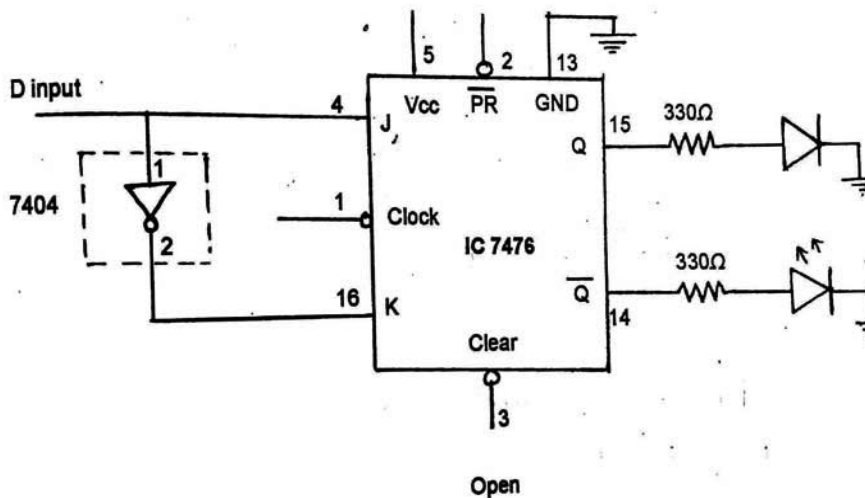


Figure 12.3 D FF using 7476

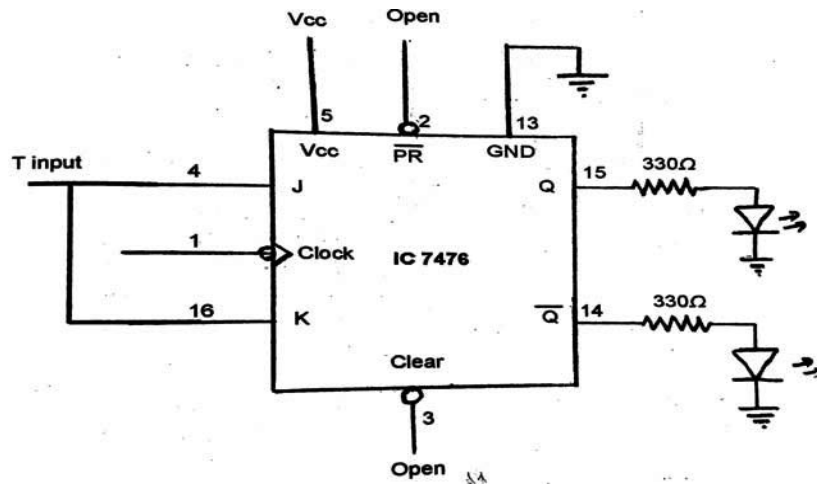


Figure 12.4 T FF using 7476

a) Actual Circuit used in laboratory

b) Actual Experimental set up used in laboratory

X Resources Required

S. No.	Instrument /Components	Specification	Quantity	Remarks
1	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	7476	1	
6	LED	Red /Yellow color 5 mm	2	
7	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8	Resistors	330Ω	2	

XI Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XII Procedure

1. Mount the IC7476 on the breadboard.
2. Make the connections as shown in figure 12.3 and 12.4
3. Apply the supply voltage to IC +5V.
4. Apply inputs according to the observation table.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

XIII Resources used (with major specifications)

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIV Actual procedure followed (Use blank sheet provided if space not sufficient)

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XV Precautions followed (Use blank sheet provided if space not sufficient)

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XVI Observations and Calculations

Table 3: Truth Table D, T flip-flop

Input D	Output Q_{n+1}
0	
1	

Input T	Output Q_{n+1}
0	
1	

XVII Results

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XVIII Interpretation of results (Give meaning of the above obtained results)

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XIX Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

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XX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

1. List the name of manufacturer of Digital IC used in practical.
2. What is the function of IC 7474 draw its pin diagram?

[Space for answer]

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XX References / Suggestions for further reading

1. www.alldatasheet.com/datasheet-pdf
2. <http://www.electronics-tutorials.ws>

XXI Suggested Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.13: 4 bit ripple counter.

I Practical Significance:

Counter is a sequential circuit used for counting the number of clock pulses. It is a group of Flip-Flops with a clock signal applied to it. A counter has natural count of 2^n where “n” is number of flip-flops in the counter. A 4-bit counter has 16 states.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer engg. knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: ‘**Build/ test digital logic circuits using digital ICs**’

- i. Identify pin configuration for IC.
- ii. Make relevant connections as per circuit diagram.

IV Relevant Course Outcome(s)

- Build simple Sequential circuits.

V Practical Outcome:

- Implement 4 bit ripple counter using 7476.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

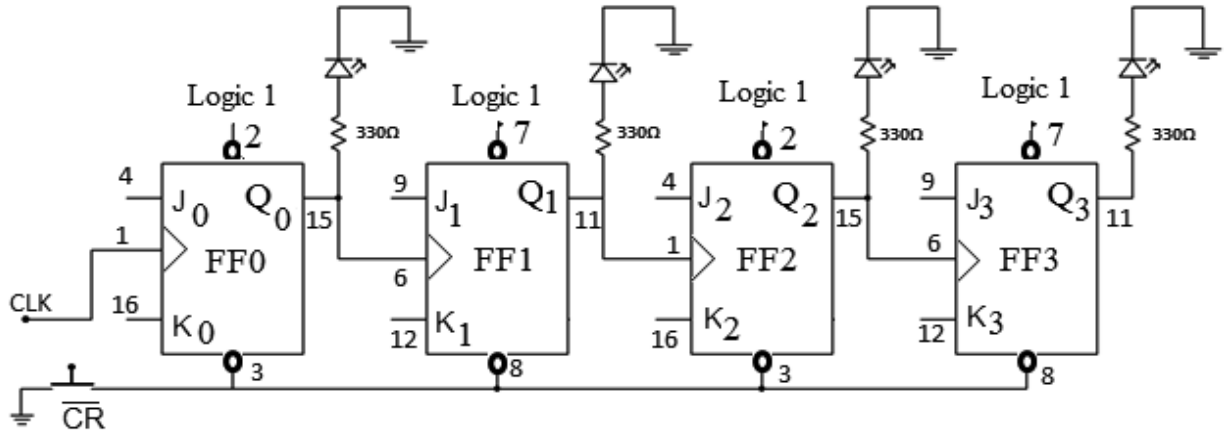
VII Minimum Theoretical Background:

A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples away through the flip-flops. When decimal equivalent of the counter output increases as it receives the clock pulses, then that counter is known as Up Counter. When decimal equivalent of the counter output decreases as it receives the clock pulses, then that counter is known as Down Counter.

VIII Practical set-up / Circuit diagram

a) Sample

4-BIT Asynchronous counter



(J, K, PR terminals are kept open which act as high for TTL IC)

Figure.13.1 bit Ripple Counter using J-K flip flop

b) Actual Experimental set up used in laboratory

c) Actual Experimental set up used in laboratory

IX Resources Required

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1	Digital Multimeter	Digital Multimeter:3 ½ digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboard	5.5cm X 17 cm	1	
4	DC power supply	+5 V Fixed power supply	1	
5	Clock Pulse	Function/Pulse Generator	1	
6	IC 1	7476	2	
7	LED	Red /Yellow color 5 mm	4	
8	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
9	Resistors	330 Ω /0.25 W	4	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Connect +5V Power supply to proper pins of IC.
2. Connect appropriate resistor and LED to output Q.
3. Clear all the flip-flops by applying active low input to the clear pin so that the flip-flops have 0000 stored in them.
4. Apply clock pulse at clock input and after every clock pulse write down the counter output state from LED (ON LED =1 State, OFF LED =0 State)
5. Apply 16 clock pulses and write down the output of counter in truth table.

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

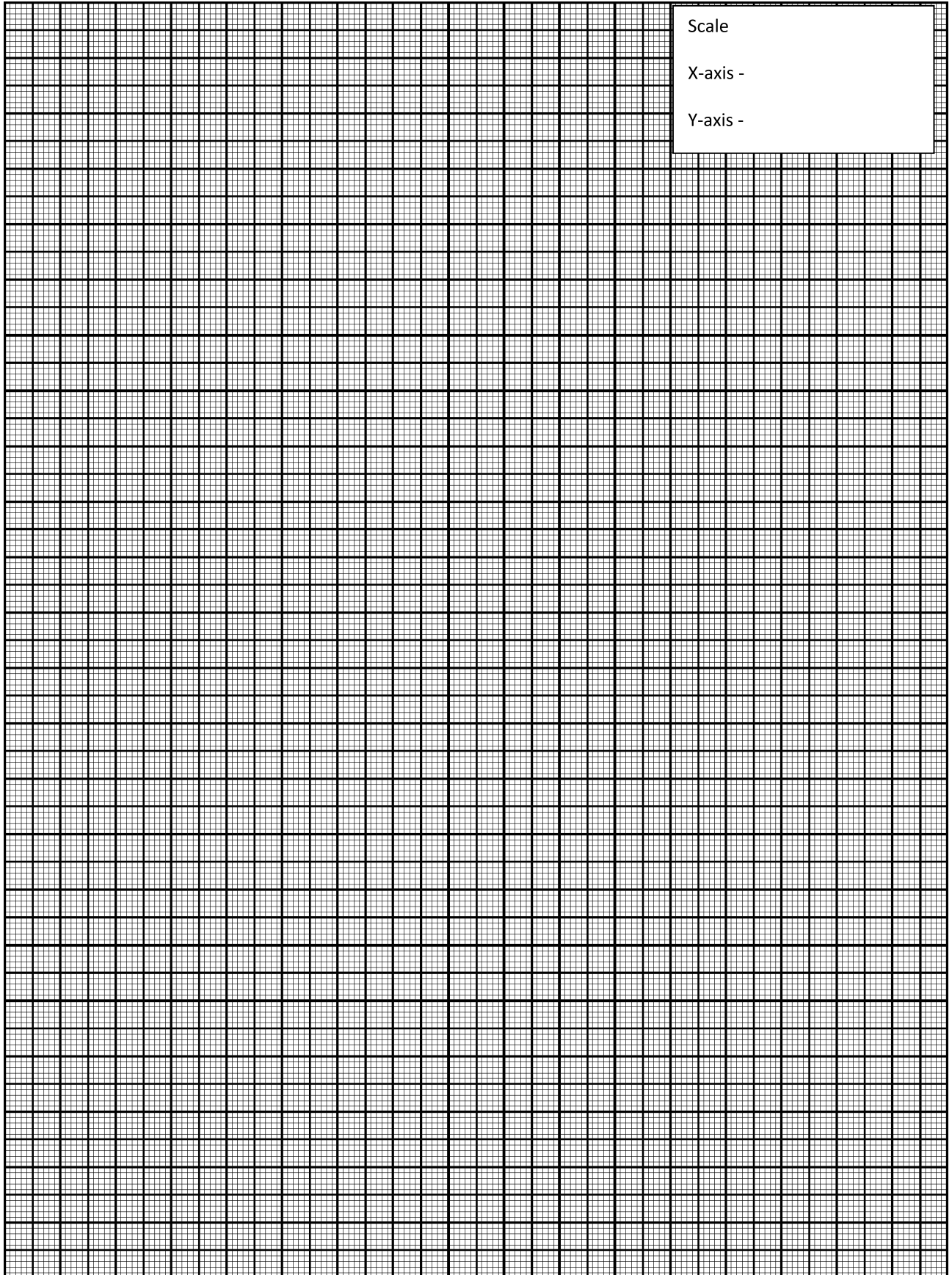
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XIV Precautions Followed (Use blank sheet provided if space not sufficient)

- 1
- 2

XV Observations and Calculations:**Observation Table for 4-BIT Asynchronous Up counter**

Input No. of clock pulses	Output				Decimal Equivalent
	Q ₃	Q ₂	Q ₁	Q ₀	
0					
1					
2					
3					
4					
5					
6					
7					
8					
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12					
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15					
16					



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XX References / Suggestions for further reading

1. <https://www.eecs.tufts.edu/~dsculley/tutorial/flopsandcounters/flops6.html>
2. www.falstad.com/circuit/e-counter.html
3. <https://www.electronicshub.org> › Counters

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Test the IC's using IC tester	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.14: Decade counter using IC 7490.

I Practical Significance:

Counter is a sequential circuit used for counting the number of clock pulses. It is a group of Flip-Flops with a clock signal applied to it. A counter has natural count of 2^n where “n” is number of flip-flop in the counter. Decade counter is a counter which has ten states from 0 to 9.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: **‘Build/ test digital logic circuits using digital ICs.**

- i. Identify pin configuration for IC
- ii. Make connections as per circuit diagram.

IV Relevant Course Outcome(s)

- Build simple sequential circuits.

V Practical Outcome

- Use IC 7490 to construct decade counter (MOD-10).

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background:

- Decade counter is the one that goes through 10 unique combinations of output and then resets as the clock proceeds further. Since it is MOD -10 counters, it can be constructed with a minimum of four flip-flops. A four bit counter would have 16 states. By skipping any of six states by using some kind of feedback or some kind of additional logic, we can convert a normal four bit binary counter into a decade counter.
- IC 7490 is a BCD asynchronous counter. It consists of 4 flip flops, internally connected so as to provide Mod-2 and Mod -5 counter functions. These ICs have set and reset inputs. These inputs help in designing a modulus –M counter. The Mod -2 and Mod -5 counters can be used independently or in combinations. Flip flop FFA operates as a mod-2 counter whereas the combination of flip flops FFB, FFC, and FFD form a mod-5 counter. There are two reset inputs R1 and R2 both of which are to be connected to logic 1 level to reset the flip flops. The two set inputs S1 and S2, when connected to logic 1 level, are used for setting the counter to 1001. for normal operation set and rest inputs are connected to 0.

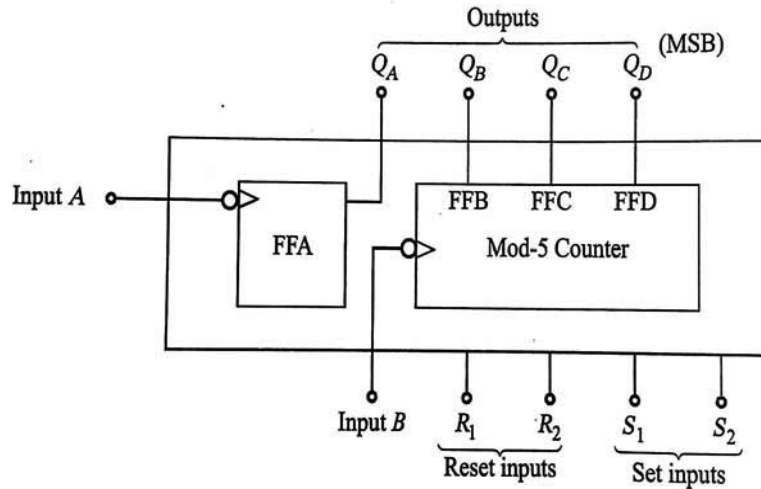


Figure 14.1 Block diagram of IC 7490

VIII Practical set-up / Circuit diagram
a) Sample

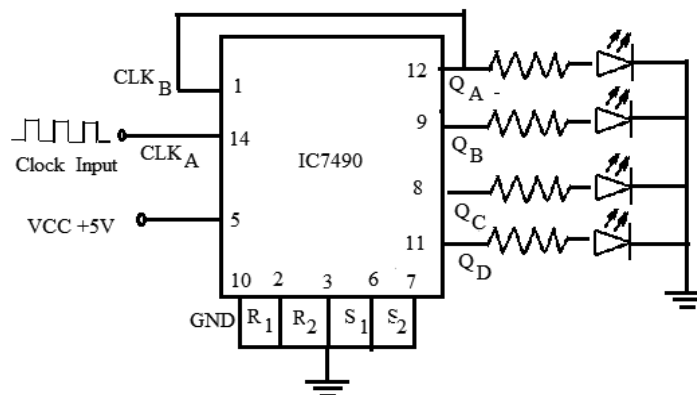


Figure 14.2 Decade Counter using 7490

CKB	1	14	CKA
R0(1)	2	13	NC
R0(2)	3	12	QA
NC	4	11	QD
Vcc	5	10	GND
R9(1)	6	9	QB
R9(2)	7	8	QC

Pin	Symbol	Description
1	CKB	clock input
2	R0(1)	reset to 0
3	R0(2)	reset to 0
4	NC	no connection
5	Vcc	supply voltage
6	R9(1)	reset to 9
7	R9(2)	reset to 9
8	QC	counter output
9	QB	counter output
10	GND	ground
11	QD	counter output
12	QA	counter output
13	NC	no connection
14	CKA	clock input

Figure 14.3 Pin Configuration of IC 7490

b) Actual circuit used in laboratory**c) Actual Experimental set up used in laboratory****IX Resources Required**

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1	Digital Multimeter	Digital Multimeter:3 ½ digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboard	5.5cm X 17 cm	1	
4	DC power supply	+5 V Fixed power supply	1	
5	IC 1	7490	1	
6	Clock pulse	Function/pulse generator	1	
7	LED	Red /Yellow color 5 mm	4	
8	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
9	Resistors	330 Ω	4	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

- 1) Mount IC 7490 on breadboard
- 2) Make the connection for given circuit diagram.(figure 14.2)
- 3) Apply the clock input.
- 4) Observe and record the outputs on LEDs (ON/OFF).

XII Resources Used

Sr. No.	Instrument /Components	Specification	Quantity

XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

1.
2.

XIV Precautions Followed (Use blank sheet provided if space not sufficient)

1.
2.

**XV Observations and Calculations:
Observation Table for Decade Counter**

Input No. of clock pulses	Output				Decimal Equivalent
	Q _D	Q _C	Q _B	Q _A	
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

XVI Results

1.
2.

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XX References / Suggestions for further reading

1. <https://www.eecs.tufts.edu/~dsculley/tutorial/flopsandcounters/flops6.html>
2. www.falstad.com/circuit/e-counter.html
3. <https://www.electronicshub.org> > Counters

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Test the IC's using IC tester	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.15: 4 Bit Universal Shift Register.

I Practical Significance:

Universal Shift Register is a register which can be configured to load and/or retrieve the data in any mode (either serial or parallel) by shifting it either towards right or towards left. In other words, a combined design of unidirectional (either right- or left-shift of data bits as in case of SISO, SIPO, PISO, PIPO) and bidirectional shift register along with parallel load provision is referred to as universal shift register.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: '**Build/ test digital logic circuits using digital ICs**'.

- i. Identify pin configuration for IC
- ii. Make relevant connections as per circuit diagram.
- iii. Handle components/ICs.

IV Relevant Course Outcome(s)

- Build simple Sequential circuits.

V Practical Outcome:

- Build/test 4 bit universal shift register.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background:

A unidirectional shift register is a register that is capable of transferring data in only one direction. Whereas the register that is capable of transferring data in both left and right direction is called a 'bidirectional shift register.' Now let we have a register which can be capable to transfer data in both the shift-right and shift-left, along with the necessary input and output terminals for parallel transfer, then it is called a *shift register* with *parallel load* or 'universal shift register.'

Various control Functions in shift registers are as below.

1. A shift-right control to enable the shift-right operation and the serial input and output lines associated with the shift-right.
2. A shift-left control to enable the shift-left operation and the serial input and output lines associated with the shift-left.
3. A parallel-load control to enable a parallel transfer and the n input lines associated with the parallel transfer.
4. n parallel output lines.

5. A clear control to clear the register to 0.
6. A *CLK* input for clock pulses to synchronize all operations.

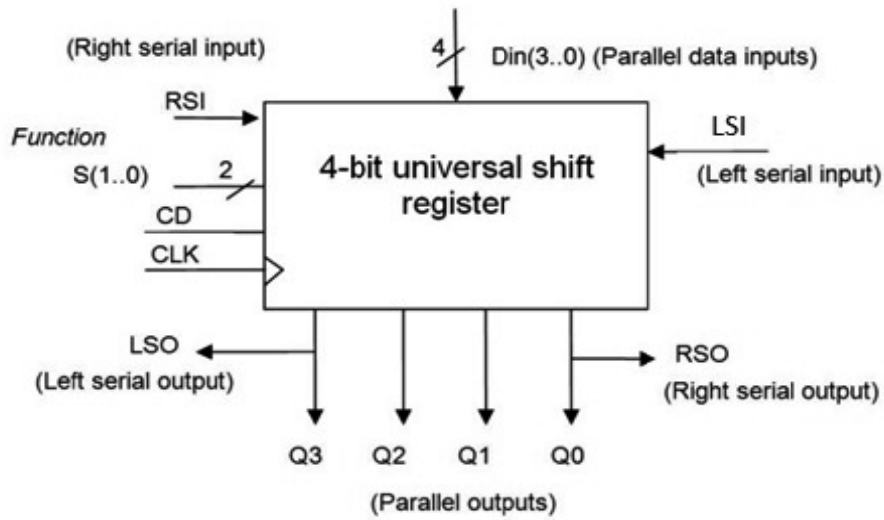


Fig 15.1

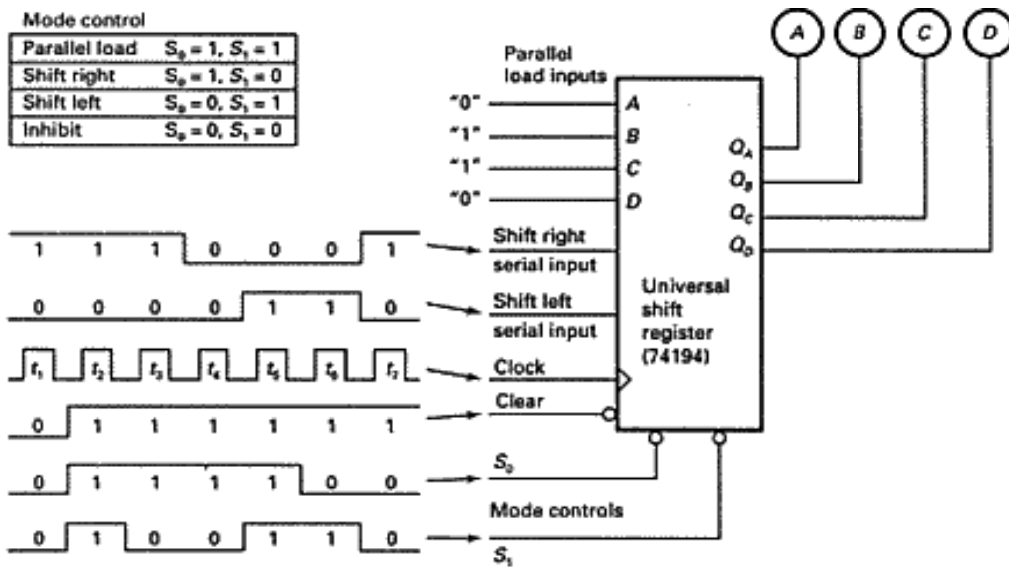


Fig.15.2

VIII Practical set-up / Circuit diagram

a) Sample

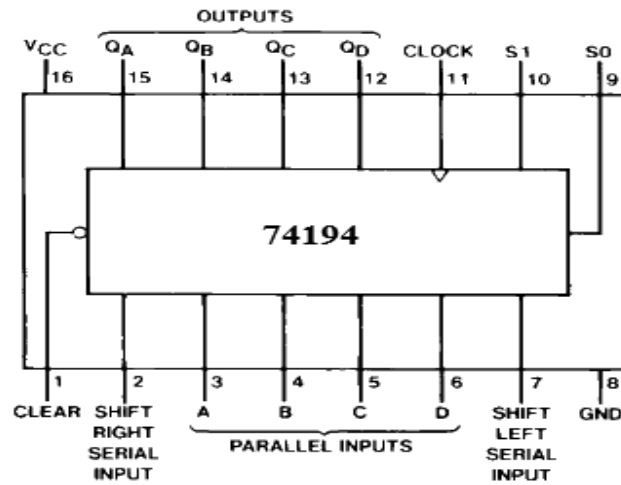


Figure 15.3 Universal Shift Register

b) Actual circuit used in laboratory

c) Experimental set up used in laboratory

IX Resources Required

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1	Digital Multimeter	Digital Multimeter:3 ½ digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboard	5.5cm X 17 cm	1	
4	DC power supply	+5 V Fixed power supply	1	
5	Clock Pulse	Function/Pulse Generator	1	
6	IC 1	74194	1	
7	LED	Red /Yellow color 5 mm	4	
9	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
10	Resistors	330 Ω/0.25 W	4	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Connect appropriate resistor and LED to output Q.
2. Clear all the flip-flops by applying active low input to the clear pin so that the flip-flops have 0000 stored in them.
3. Apply clock pulse one by one to clock input.
5. Connect input and observe output for all modes.
7. Write down observation table.

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

1.
2.

XIV Precautions Followed (Use blank sheet provided if space not sufficient)

1.
2.

XV Observations and Calculations:

1.
2.

Observation Table for Right Shift Operation:

Clock pulses	Theoretical				Practical			
	Q ₃	Q ₂	Q ₁	Q ₀	Q ₃	Q ₂	Q ₁	Q ₀
0								
1								
2								
3								
4								

In SISO mode o/p is taken at Q₀, In SIPO mode o/p is taken at Q₃, Q₂, Q₁, Q₀ simultaneously.

XVI Results

1.
2.

XVII Interpretation of Results (Give meaning of the above obtained results)

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XVIII Conclusions and recommendations (Actions/decisions to be taken based on the interpretation of results).

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XIX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

1. State the operation for PIPO and PISO.
2. Draw observation table for above operation.
3. Build circuit for SISO, SIPO, PIPO, and PISO separately.
4. Draw timing diagram for SIPO.

[Space for Answers]

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XX References / Suggestions for further reading

1. www.sycelectronica.com.ar/semiconductores/74LS194.pdf
2. www.esi.uclm.es/www/isanchez/apuntes/ci/74194.pdf
3. https://www.electronics-tutorials.ws/sequential/seq_5.html

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Testing of IC's using IC tester	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

Practical No.16: R-2R resistive network.

I Practical Significance: A digital to analog converter (DAC) is a circuit that converts digital numbers into analog voltage or current output. R-2R ladder is a resistive network of which output voltage is a properly weighted sum of the digital inputs. With this experiment you will get an exposure to R-2R network which is used in digital to analog converters.

II Relevant Program Outcomes (POs)

1. **Discipline knowledge:** Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
2. **Experiments and practice:** Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. **Engineering tools:** Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: ‘**Build/ test digital logic circuits using digital ICs**’.

- i. Identify pin configuration for IC.
- ii. Make relevant connections as per circuit diagram.
- iii. Handle components/ICs.

IV Relevant Course Outcome(s)

- Test digital to analog converters in digital electronics systems.

V Practical Outcome:

- Build R-2R resistive network on breadboard to convert given digital data into analog.

VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

VII Minimum Theoretical Background:

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin’s theorem in arriving at the desired output voltages. The R-2R network consists of resistors with only two values - R and 2R. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. This is elaborated in fig.16.1.

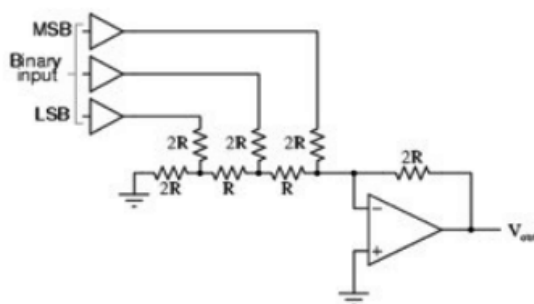
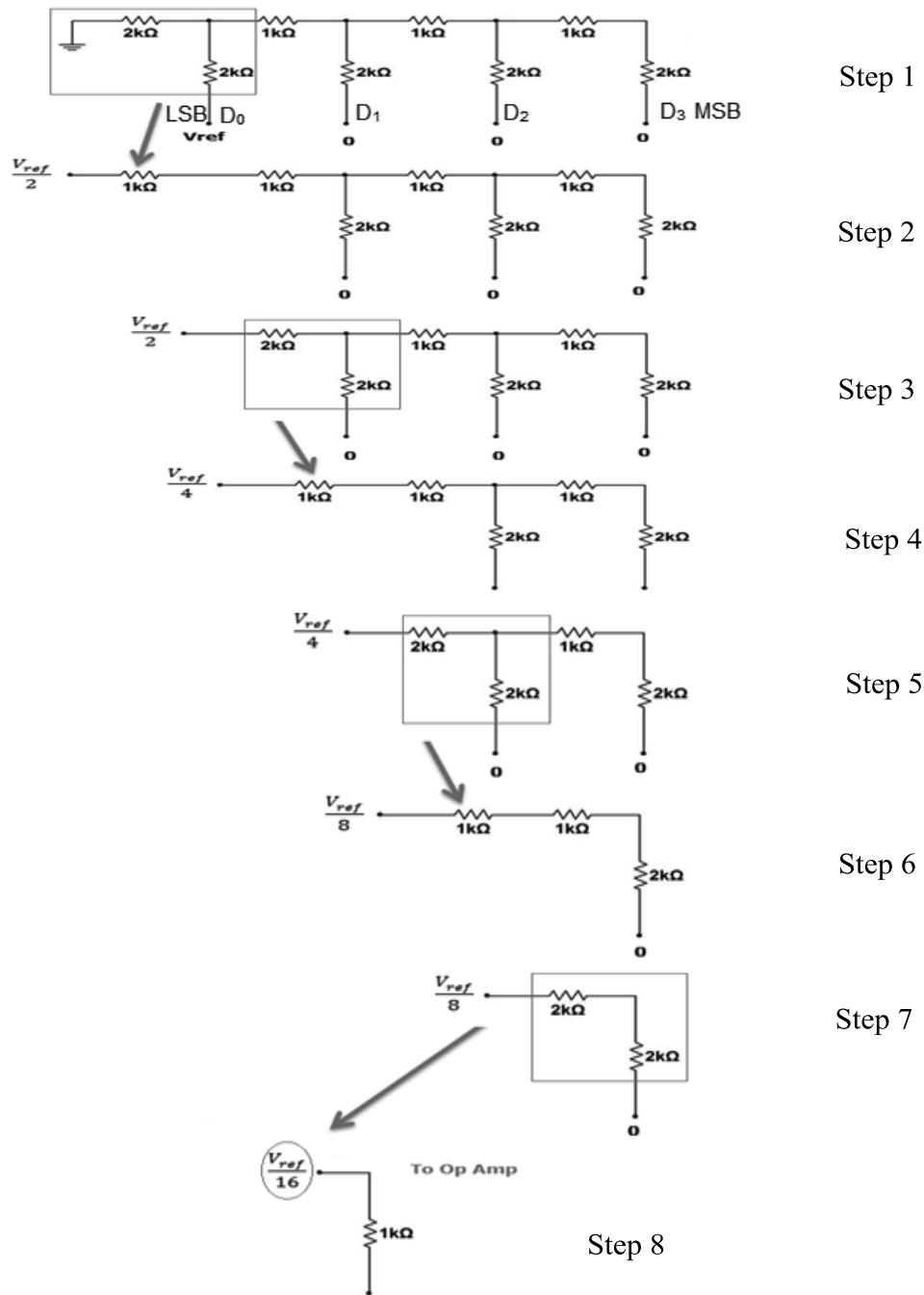


Figure 16.1: Basic diagram of R-2R ladder network working of R-2R ladder network DAC

- R-2R weighted resistor ladder network uses only 2 set of resistors- R and 2R. If you want to build a very precise DAC, be precise while choosing the values of resistors that will exactly match the R-2R ratio.
- This is a 4 bit DAC. Let us consider the digital data $D_3D_2D_1D_0=0001$ is applied to the DAC, then the Thevenin equivalent circuit reduction is shown below.



- V_{ref} is nothing but the input binary value reference voltage, that is for binary 1, $V_{ref}=5V$ and for binary 0, $V_{ref}=0V$.
- For 0001 only $D_0=V_{ref}$, all other inputs are at 0V and can be treated as ground. So finally $V_{ref}/16$ volt is appearing as the input to op amp. This value gets multiplied by the gain of op amp circuit – (R_f/R_i) .

- If we proceed in this manner (Thevenin equivalent reduction), we will get

$$V_{out} = -\frac{R_f}{R_i} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

- Note that you can build a DAC with any number of bits you want, by simply enlarging the resistor network, by adding more R-2R resistor branches.

VIII Practical set-up / Circuit diagram

a) Sample

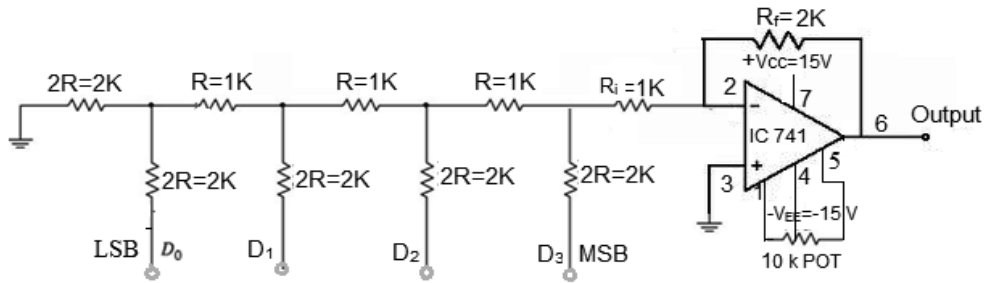


Figure 16.2 R-2R Ladder D/A Network

b) Actual circuit Experimental set up used in laboratory

c) Actual circuit Experimental set up used in laboratory**IX Resources Required**

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1	Digital Multimeter	Digital Multimeter:3 ½ digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboards	5.5cm X 17 cm	1	
4	DC power supply	+5 V Fixed power supply,+/-15 V	1	
5	Clock Pulse	Function/Pulse Generator	1	
6	IC 1	7493	1	
7	IC 2	741	1	
8	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
9	Potentiometer	10KΩ	1	
10	Resistors	1KΩ and 2KΩ	6 (2 KΩ) 4 (1KΩ)	

X Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure:

1. Test IC using IC tester.
2. Mount IC on bread board.
3. Build circuit as per circuit diagram.
4. Write down observation table.
5. With all inputs (D0 to D3) shorted to ground, adjust the 10KΩ POT until the output is 0V. This will nullify any offset voltage at the input of the OPAMP. (POT connected between pin 1 & pin 5 of OP-AMP)
6. Measure the output voltage for all binary input states. (0000 to 1111).

XII Resources Used

S. No.	Instrument /Components	Specification	Quantity
1.			
2.			
3.			
4.			
5.			

XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

1.
2.

XIV Precautions Followed

1.
2.

XV Observations and Calculations:

Observation Table for R-2R Ladder DAC:

D ₃	D ₂	D ₁	D ₀	R-2R Ladder DAC	
				Theoretical (V) $V_0 = \frac{R_f}{R_i} V_{ref} \left(\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right)$	Practical (V)
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

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XX References / Suggestions for further reading

1. <http://www.circuitgallery.com/2012/04/digital-to-analog-converter-using-r-2r.html>
2. www.idconline.com/technical_references/pdfs/electronic.../R_2_R_Ladder_DAC.pdf
3. www.circuitgallery.com/2012/04/digital-to-analog-converter-using-r-2r.html

XXI Assessment Scheme

Performance indicators		Weightage
Process related:15 Marks		60%
1	Testing of IC's using IC tester	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05%
Total (25 Marks)		100 %

Names of Student Team Members

1.
2.
3.
4.

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

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1	Fundamentals of ICT	22001
2	English	22101
3	English Work Book	22101
4	Basic Science (Chemistry)	22102
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Second Semester:

1	Business Communication Using Computers	22009
2	Computer Peripherals & Hardware Maintenance	22013
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19	Fundamentals Of Mechatronics	22048

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12	System Programming	17634
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15	Illumination Engineering	17639
16	Power System Operation & Control	17643
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25	Video Engineering	17668
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28	Intensive Care Equipment	17672
29	Medical Imaging Equipment	17673

Pharmacy Lab Manual

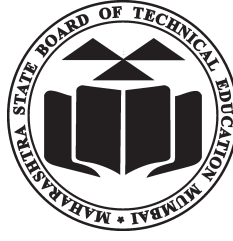
First Year:

1	Pharmaceutics - I	0805
2	Pharmaceutical Chemistry - I	0806
3	Pharmacognosy	0807
4	Biochemistry and Clinical Pathology	0808
5	Human Anatomy and Physiology	0809

Second Year:

1	Pharmaceutics - II	0811
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