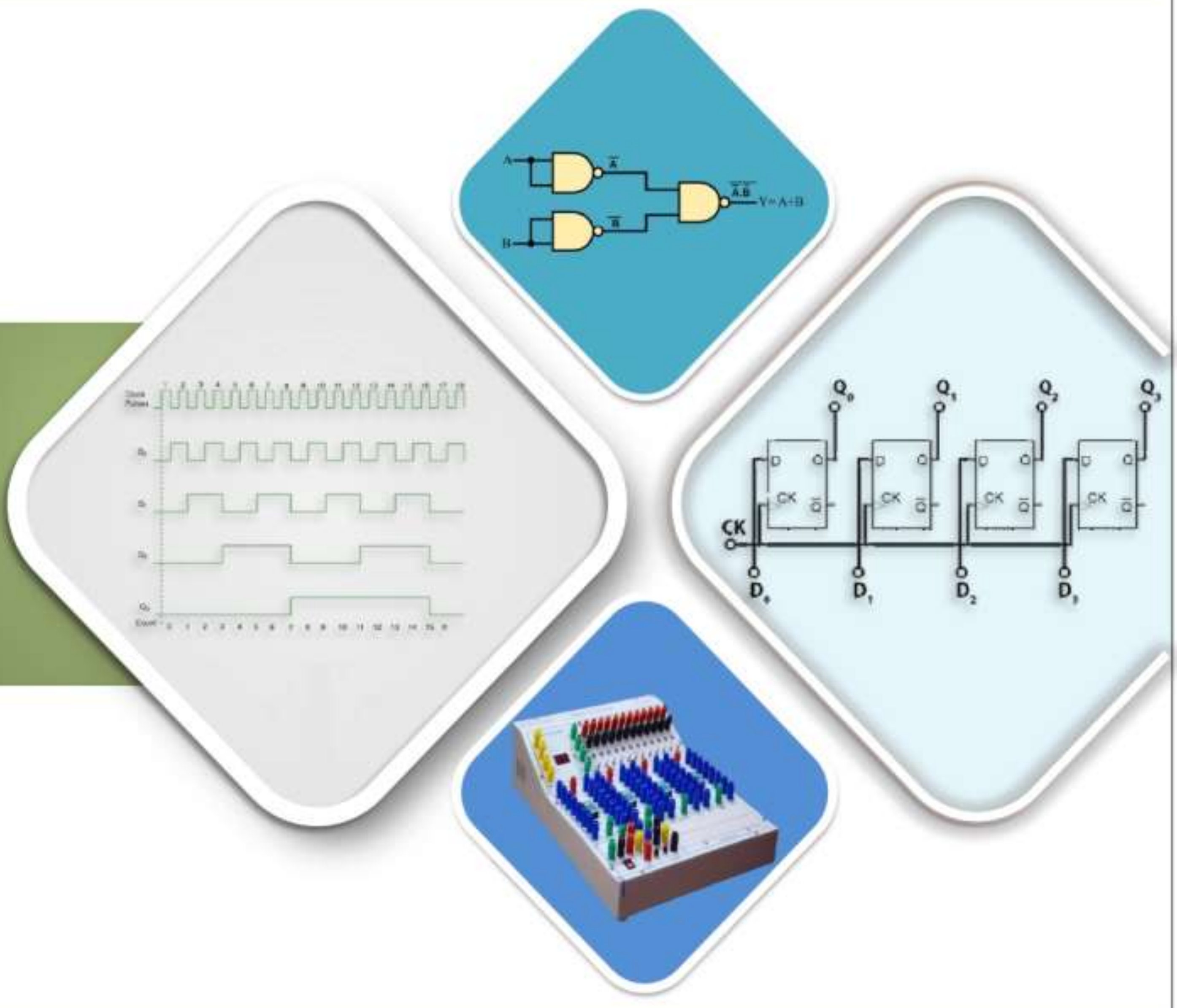
**SCHEME : K**

Name : ______________________________

Roll No. : ________________ Year : 20___ 20___

Exam Seat No. : ______________________

# LABORATORY MANUAL FOR
# DIGITAL TECHNIQUES
# (313303)




**COMPUTER / ELECTRONICS ENGINEERING GROUP**


**MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION, MUMBAI**

**(Autonomous) (ISO 9001: 2015) (ISO/IEC 27001:2013)**

## VISION

To ensure that the Diploma level Technical Education constantly matches the latest requirements of Technology and industry and includes the all-round personal development of students including social concerns and to become globally competitive, technology led organization.

## MISSION

To provide high quality technical and managerial manpower, information and consultancy services to the industry and community to enable the industry and community to face the challenging technological & environmental challenges.

## QUALITY POLICY

We, at MSBTE, are committed to offer the best in class academic services to the students and institutes to enhance the delight of industry and society. This will be achieved through continual improvement in management practices adopted in the process of curriculum design, development, implementation, evaluation and monitoring system along with adequate faculty development programmes.

## CORE VALUES

MSBTE believes in the following

- Skill development in line with industry requirements
- Industry readiness and improved employability of Diploma holders
- Synergistic relationship with industry
- Collective and Cooperative development of all stakeholders
- Technological interventions in societal development
- Access to uniform quality technical education

A Laboratory manual for

# Digital Techniques

## (313303)

## Semester – III

**(AI/AN/AO/CM/CO/CW/DE/DS/EJ/ET/EX/HA/IC/IE/ IS/MU/TE)**

## Maharashtra State

## Board of Technical Education, Mumbai

**(Autonomous) (ISO 9001:2015) (ISO/IEC 27001:2013)**

**Maharashtra State Board of Technical Education , Mumbai**
**(Autonomous) (ISO 9001:2015) (ISO/IEC 27001:2013)**
**4th Floor, Government Polytechnic Building, 49,**
**Kherwadi, Bandra (East), Mumbai- 400051.**
**(Printed on July, 2024)**

# MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION MUMBAI

## Certificate

This is to certify that Mr./Ms. ……………………………………….......... Roll No. …………. of Third Semester of Diploma in …..……………………………………….....................................of Institute …...……………………………………………………………………………... (Code : ………) has attained pre-defined practical outcomes (PROs) satisfactorily in course **Digital Techniques (313303)** for the academic year 20…... .to 20…….. as prescribed in the curriculum.

Place: …………….. Enrollment No.: ………………..

Date: ………………. Exam Seat No.: …………………

**Course Teacher** **Head of the Department** **Principal**

Seal
of
Institute

# Preface

The primary focus of any engineering laboratory/field work in the technical education system is to develop the much needed industry relevant competencies and skills. With this in view, MSBTE embarked on this innovative 'K' Scheme curricula for engineering diploma programmes with outcome-based education as the focus and accordingly, a relatively large amount of time is allotted for the practical work. This displays the great importance of laboratory work, making each teacher, instructor and student to realize that every minute of the laboratory time needs to be effectively utilized to develop these outcomes, rather than doing other mundane activities. Therefore, for the successful implementation of this outcome- based curriculum, every practical has been designed to serve as a ***'vehicle'*** to develop this industry identified competency in every student. The practical skills are difficult to develop through "chalk and duster" activity in the classroom situation. Accordingly, the "K" scheme laboratory manual development team designed the practical to focus on the outcomes, rather than the traditional age old practice of conducting practical to 'verify the theory" (which may become a byproduct along the way).

This laboratory manual is designed to help all stakeholders, especially the students, teachers and instructors to develop in the student the predetermined outcomes. It is expected. from each student that at least a day in advance, they have to thoroughly read through the concerned practical procedure that they will do the next day and understand the minimum theoretical background associated with the practical. Every practical in this manual begins by identifying the competency, industry relevant skills, course outcomes and practical outcomes which serve as a key focal point for doing the practical. The students will then become aware about the skills they will achieve through the procedure shown there and necessary precautions to be taken, which will help them to apply in solving real-world problems in their professional life.

This manual also provides guidelines to teachers and instructors to effectively facilitate student-centered lab activities through each practical exercise by arranging and managing necessary resources in order that the students follow the procedures and precautions systematically ensuring the achievement of outcomes in the students.

The basic aim of this course is that, the student must learn logic gates, combinational and sequential circuits using discrete gates and digital ICs will enable students to interpret working of digital equipment and test their functionality.

Although best possible care has been taken to check for errors (if any) in this laboratory manual, perfection may elude us as this is the first edition of this manual. Any errors and suggestions for improvement are solicited and highly welcome.

# Program Outcomes (POs)

Following programme outcomes are expected to be achieved through the practical of the course.

- **PO1: Basic and Discipline specific knowledge**: Apply knowledge of basic mathematics, science and engineering fundamentals and engineering specialization to solve the broad based Electronic Engineering group program problems.

- **PO2: Problem analysis:** Identify and analyze well-defined Electronic Engineering group program problems using codified standard methods.

- **PO3: Design/ development of solutions:** Design solutions for well-defined technical problems and assist with the design of Electronic Engineering group program systems components or processes to meet specified needs.

- **PO4: Engineering Tools, Experimentation and Testing:** Apply modern Electronic Engineering group program tools and appropriate technique to conduct standard tests and measurements.

- **PO5: Engineering practices for society, sustainability and environment:** Apply appropriate Electronic Engineering group program technology in context of society, sustainability, environment and ethical practices.

- **PO6: Project Management**: Use Electronic Engineering group program management principles individually, as a team member or a leader to manage projects and effectively communicate about well-defined engineering activities.

- **PO7: Life-long learning**: Ability to analyze individual needs and engage in updating in the context of Electronic Engineering group program technological changes.

# List of relevant expected psychomotor domain skills

The following industry relevant skills of the identified competency "test the functionality of the digital circuits/system." are expected to be developed in the student by undertaking the laboratory work as given in laboratory manual.

1. Apply number system and codes concept to interpret working of digital systems.
2. Apply Boolean laws to minimize complex Boolean functions.
3. Develop combinational logic circuits for given applications.
4. Develop sequential logic circuits using Flip-flops.
5. Interpret the functions of data converters and memories in digital electronic systems.

## Practical-Course outcome matrix

**COURSE LEVEL LEARNING OUTCOMES (COS)**

CO1 - Apply number system and codes concept to interpret working of digital systems.
CO2 - Apply Boolean laws to minimize complex Boolean functions.
CO3 - Develop combinational logic circuits for given applications.
CO4 - Develop sequential logic circuits using Flip-flops.
CO5 - Interpret the functions of data converters and memories in digital electronic systems.

| Sr. No. | Title of the Practical | CO1 | CO2 | CO3 | CO4 | CO5 |
|---|---|---|---|---|---|---|
| 1 | Test the functionality of AND, OR, NOT, EX-OR and EX-NOR logic gates using equivalent 74 series or CMOS Devices (CD) Series | ✓ | ✓ | — | — | — |
| 2 | Test the functionality of the given universal gates using equivalent 74 series/CD series | — | ✓ | — | — | — |
| 3 | Construct Basic gates using Universal Gates | — | ✓ | — | — | — |
| 4 | Construct Exclusive Gates using Universal gates | — | ✓ | — | — | — |
| 5 | Verify De-Morgan’s Theorem (1 and 2) | — | ✓ | — | — | — |
| 6 | Implement 2 input, 3 input Adder Circuit | — | — | ✓ | — | — |
| 7 | Implement 2 input, 3 input Subtractor Circuit | — | — | ✓ | — | — |
| 8 | Test the output of BCD to 7 segment Decoder using Digital IC for the given inputs | — | — | ✓ | — | — |
| 9 | Checks the output of comparator circuit consist of Digital IC. | — | — | ✓ | — | — |
| 10 | Build and test the functionality of 4:1/8:1 Multiplexer | — | — | ✓ | — | — |
| 11 | Build and test the functionality of 1:4/1:8 Demultiplexer | — | — | ✓ | — | — |
| 12 | Implement and Verify the truth table of RS Flipflop | — | — | — | ✓ | — |
| 13 | Implement and Test the functionality of Master Slave JK Flip Flop using Digital IC | — | — | — | ✓ | — |
| 14 | Use Digital IC to construct and Test the functionality of D and T flip flop | — | — | — | ✓ | — |
| 15 | Build 4- bit Universal Shift register and Observe the timing Diagram | — | — | — | ✓ | — |

## Practical-Course outcome matrix

**COURSE LEVEL LEARNING OUTCOMES (COS)**

CO1 - Apply number system and codes concept to interpret working of digital systems.
CO2 - Apply Boolean laws to minimize complex Boolean functions.
CO3 - Develop combinational logic circuits for given applications.
CO4 - Develop sequential logic circuits using Flip-flops.
CO5 - Interpret the functions of data converters and memories in digital electronic systems.

| Sr. No. | Title of the Practical | CO1 | CO2 | CO3 | CO4 | CO5 |
|---|---|---|---|---|---|---|
| 16 | Implement Ripple counter using Digital IC | — | — | — | ✓ | — |
| 17 | Implement Decade Counter using Digital IC | — | — | — | ✓ | — |
| 18 | Test the output of given R-2R type Digital to Analog Converter for the given input | — | — | — | — | ✓ |

# Guidelines to Teachers

1. Teacher should provide the guideline with demonstration of practical to the students with all features.
2. Teacher shall explain prior concepts to the students before starting of each practical.
3. Involve students in the performance of each experiment.
4. Teacher should ensure that the respective skills and competencies are developed in the students after the completion of the practical exercise.
5. Teachers should give opportunities to students for hands-on experience after the demonstration.
6. Teacher is expected to share the skills and competencies to be developed in the students.
7. Teacher may provide additional knowledge and skills to the students even though not covered in the manual but are expected of the students by the industry.
8. Finally give practical assignments and assess the performance of students based on tasks assigned to check whether it is as per the instructions.
9. Teacher is expected to refer complete curriculum document and follow guidelines for implementation.
10. At the beginning of the practical which is based on the simulation, teacher should make the students acquainted with any simulation software environment.

# Instructions for Students

1. Listen carefully the lecture given by teacher about course, curriculum, learning structure, skills to be developed.
2. Organize the work in the group and make record all observation.
3. Do the calculation and plot the graph where ever it is required in the practicals.
4. Students shall develop maintenance skill as expected by industries.
5. Student shall attempt to develop related hand-on skills and gain confidence.
6. Student shall develop the habits of evolving more ideas, innovations, skills etc. those included in scope of manual
7. Student should develop habit to submit the practicals on date and time.
8. Student should prepare well while submitting write-up of exercise.
   Attach / separate papers wherever necessary.

## Content Page

List of Practical's and Progressive Assessment Sheet

| Sr. No. | Title of the Practical | Page no. | Date of Performance | Date of Submission | Assessment Marks (25) | Dated sign. of Teacher | Remarks If any) |
|---|---|---|---|---|---|---|---|
| 15 | Build 4- bit Universal Shift register and Observe the timing Diagram | 96 | | | | | |
| 16 | Implement Ripple counter using Digital IC | 105 | | | | | |
| 17 | *Implement Decade Counter using Digital IC | 112 | | | | | |
| 18 | *Test the output of given R-2R type Digital to Analog Converter for the given input | 119 | | | | | |
| | **Total** | | | | | | |

**Note: Out of above suggestive LLOs -**

- '*' Marked Practicals (LLOs) are mandatory.
- Minimum 80% of above list of lab experiment are to be performed.
- Judicial mix of LLOs are to be performed to achieve desired outcomes.

**Practical No.1: Test the functionality of AND, OR, NOT, EX- OR and EX-NOR logic Gates using equivalent 74 series or CMOS Devices (CD) series.**

**I Practical Significance**

Logic gates are commonly referred to as the fundamental building blocks of digital circuits. Digital gates are used in all digital circuits such as switches, memories, microprocessors, and embedded systems. Knowledge of functions of logic gates will help the students to build the digital circuits.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Apply Boolean laws to minimize complex Boolean function.

**IV Laboratory Learning Outcome(s):**

1. Test the functionality of basic gates.
2. Test the functionality of special purpose gates.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

**VI Relevant Theoretical Background**

A logic gate is an electronic circuit which makes logical decisions. A logic gate is basically an electronic circuit designed by using components like diodes, transistors, resistors, capacitors, etc. and capable of performing logical operations. It has only one output and one or many inputs.


**Fig. 1.1 Block diagram of logic gate**

The output of a logic gate depends on the combination of inputs and the logical operation that the logic gate performs. Logic gates are the basic building blocks of all digital systems. These gates are AND, OR, NOT, NAND, NOR, EX-OR and EX-NOR gates. In digital logic design only two voltage levels or states are applied as input, and these states are generally referred to as Logic “1” and Logic “0”, High and Low, or True and False. These two states are represented in truth tables as binary digits “1” and “0” respectively.

**Classification of Logic Gates:**

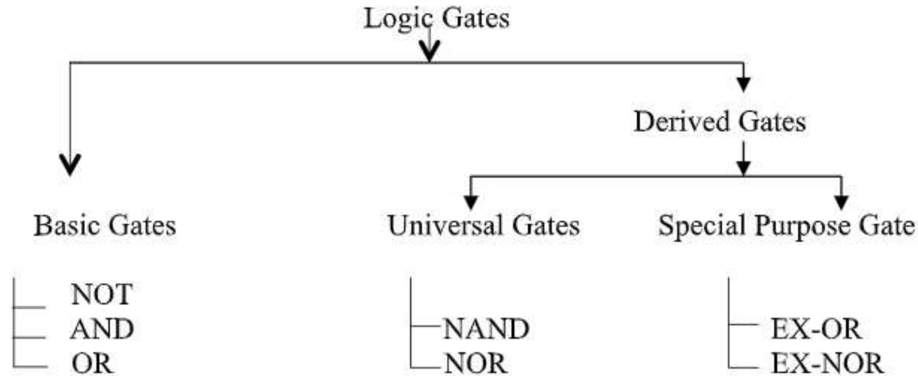



**Fig 1.2 Classification of logic gates**

**VII Circuit diagram**

**a) Sample circuit**

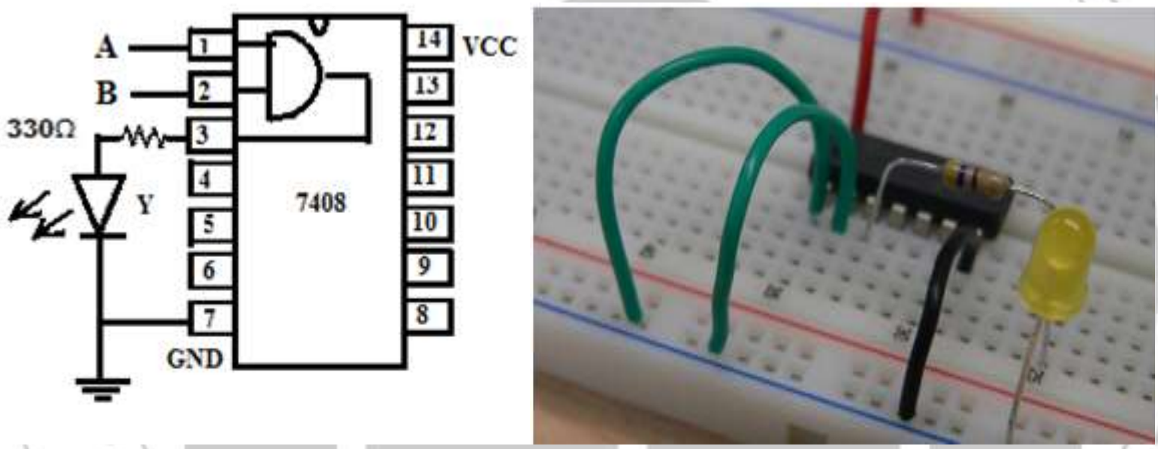



**Fig 1.3: Circuit Diagram**

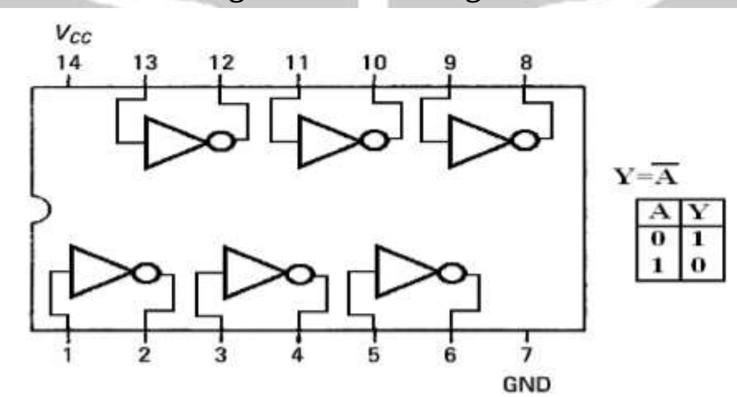



**Fig. 1.4 NOT Gate IC 7404 and truth table**

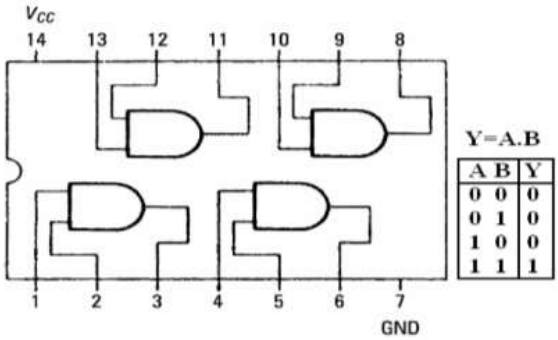



**Fig. 1.5 AND gate IC 7408 and truth table**

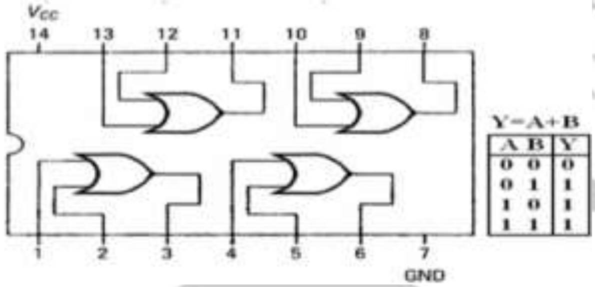



**Fig. 1.6 OR Gate IC 7432 and truth table**

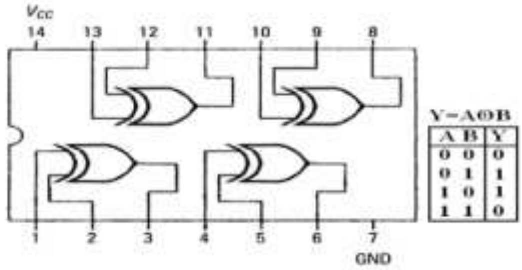



**Fig. 1.7 EX-OR Gate IC 7486 and truth table**

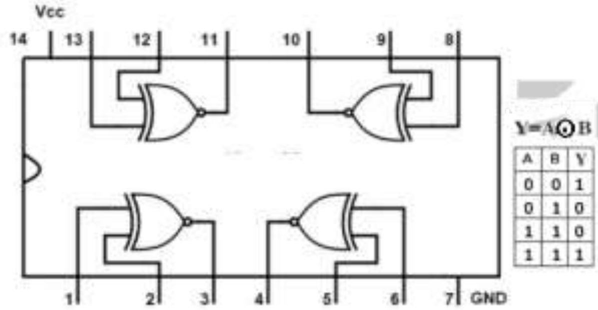



**Fig. 1.8 EX-NOR Gate IC 74266 and truth table**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 ½ digit display. | 1 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7404, 7432, 7408,7486,74266 or (CMOS IC's 4049, 4081, 4071, 4070, 4077) | 1 each |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1.1 KΩ or 330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram.

## X Procedure

1. Test the IC 7408 using Digital IC tester
2. Mount the IC on the breadboard
3. Make the connection as per fig 1.3.
4. Connect the +5V to +Vcc pin of IC and GND pin to ground
5. Observe the LED (on or off) for each combination of input as per truth table
6. Verify the truth table.
7. Repeat the process for IC 7404, 7432, 7486, 74266.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure

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## XIII Observation:

**Table 1.1: Observation Table for NOT gate**

| Input | 7404 ( NOT) | | |
|---|---|---|---|
| A | LED Status (ON/OFF) | Logic Level (1/0) | Output voltage (v) |
| 0 (0V) | | | |
| 1 (5V) | | | |

**Table 1.2: Observation Table for AND, OR, EX-OR, EX-NOR gate**

| Inputs | | 7408 ( AND) | | | 7432(OR) | | | 7486(EX-OR) | | | 74266(EX-NOR) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | LED Status (ON/OFF) | Logic Level (1/0) | Output voltage (v) | LED Status (ON/OFF) | Logic Level (1/0) | Output voltage (V) | LED Status (ON/OFF) | Logic Level (1/0) | Output voltage (V) | LED Status (ON/OFF) | Logic Level (1/0) | Output voltage (V) |
| 0(0V) | 0(0V) | | | | | | | | | | | | |
| 0(0V) | 1(5V) | | | | | | | | | | | | |
| 1(5V) | 0(0V) | | | | | | | | | | | | |
| 1(5V) | 1(5V) | | | | | | | | | | | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. Write down voltage at logic level 0 and 1 for positive logic.
2. List the function of pin 7,14 of IC 7404.
3. State the effect if pin number 14 is connected to ground and pin number 7 is connected to VCC?
4. List number of OR gates are available in IC 7432.
5. State the need for the resistor connected in series with LED. Write down the value of resistor.
6. State the significance of LS of IC number 74LS00.

**[Space for Answers]**

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## XVIII References/Suggestions for further reading


1. https://de-iitr.vlabs.ac.in/exp/truth-table-gates/theory.html
2. https://www.futurlec.com/74/IC7404.shtml
3. https://www.electroschematics.com/wp-content/uploads/2013/07/7408-datasheet.pdf
4. https://www.ti.com/lit/ds/symlink/sn5432.pdf?ts=1720330546912&ref_url=https%253A%252F%252Fwww.google.com%252F
5. https://www.ntchip.com/electronics-news/ic-7486-chip
6. https://www.jameco.com/Jameco/Products/ProdDS/47360.pdf


## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | Identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

## Practical No.2: Test the functionality of the given Universal Gates using equivalent 74 series /CD series

**I Practical Significance**

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Apply Boolean laws to minimize complex Boolean function.

**IV Laboratory Learning Outcome(s):**

1.Test the functionality of NAND and NOR gate using breadboard.

**V Relevant Affective Domain related outcome(s)**

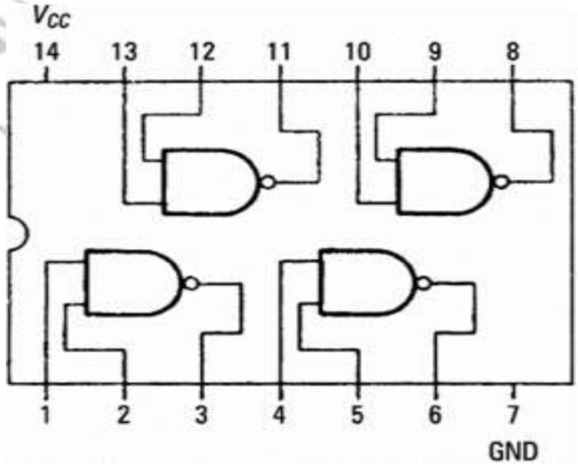
Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

**VI Relevant Theoretical Background**

OR,AND and NOT gates are the three basic logic gates as they together can be used to construct the logic circuit for any given Boolean expression. The NAND and NOR gates are known as universal gates. NOR and NAND gates have the property that they individually can be used to implement logic circuits corresponding to any given Boolean expression.

**VII Circuit diagram**

**a) Sample circuit**




$Y=\overline{A.B}$

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Fig. 2.1.NAND Gate IC 7400 and Truth table**

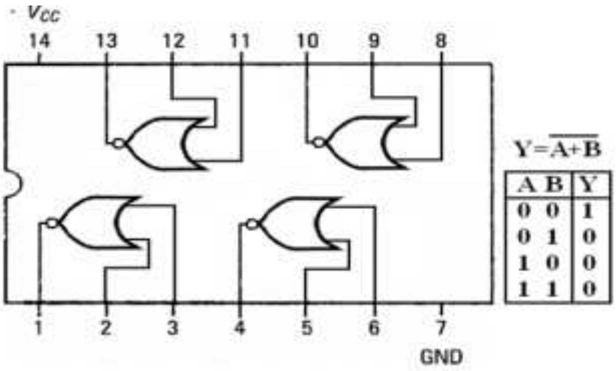



**Fig. 2.2.NOR Gate IC 7402 and Truth table**

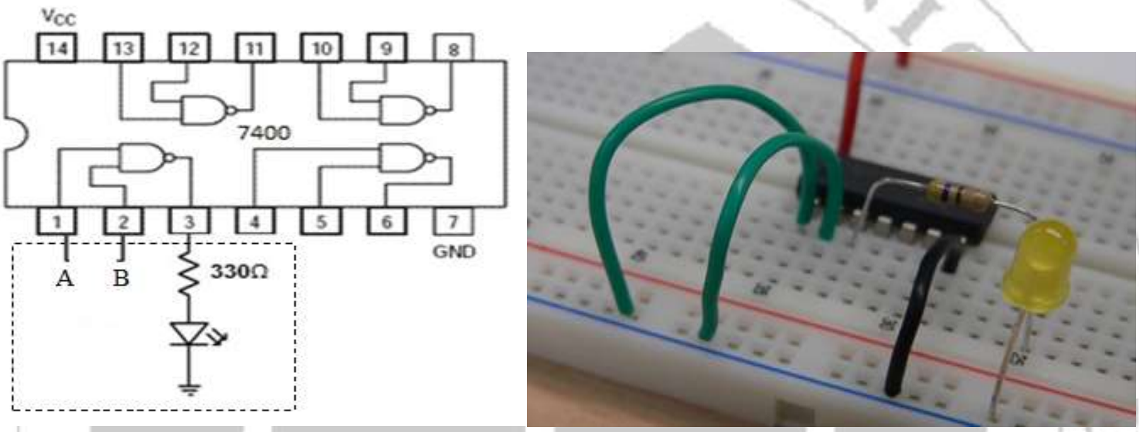



**Fig 2.3: Sample Circuit Diagram**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboards | 5.5cm X 17 cm | 1 |
| 5 | IC | 7400, 7402, or CMOS IC's.4011, 4001 | 1 Each |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1KΩ or 330Ω | As required |

## IX Precautions to be followed

1. Check IC before use.
2. Set power supply to 5V (Variable DC Power Supply) before connecting.
3. Check all the connections as per circuit diagram

## X Procedure

1. Test the IC using Digital IC tester
2. Mount the IC on the breadboard
3. Make the connection as per fig 2.3.
4. Connect the +5V to +Vcc pin of IC and GND pin to ground
5. Observe the LED (on or off) for each combination of input as per truth table
6. Verify the truth table
7. Repeat the process for IC 7402**.**

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure

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## XIII Observation:

**Table 2.1: Observation Table for NAND, NOR gate**

| Inputs | | 7400 ( NAND) | | | 7402(NOR) | | |
|---|---|---|---|---|---|---|---|
| A | B | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) |
| 0(0V) | 0(0V) | | | | | | |
| 0(0V) | 1(5V) | | | | | | |
| 1(5V) | 0(0V) | | | | | | |
| 1(5V) | 1(5V) | | | | | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. List the function of pin 7 and 14 of IC 7402.
2. Write down name of manufacturer of Digital IC 7400, 7402 used in practical.
3. Suggest another IC's used as NAND, NOR Gate.
4. Write the IC no. which has three input NAND & NOR gates.

**[Space for Answers]**

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## XVIII References/Suggestions for further reading


1. hhttps://de-iitr.vlabs.ac.in/exp/truth-table-gates/theory.html
2. https://www.futurlec.com/74/IC7400.shtml
3. https://www.futurlec.com/74/IC7402.shtml
4. https://www.youtube.com/watch?v=wn-zP-tQq5Y&list=PLUqrzxm3-gfJKoDjwuupjsFuDRm_5aVWW&index=5
5. https://www.youtube.com/watch?v=vozAQgGBetM&list=PLUqrzxm3-gfJKoDjwuupjsFuDRm_5aVWW&index=6
6. https://de-iitr.vlabs.ac.in/exp/truth-table-gates/theory.html


## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

## Practical No.3: Construct Basic Gates using Universal Gates.

**I Practical Significance**

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Apply Boolean laws to minimize complex Boolean function.

**IV Laboratory Learning Outcome(s):**

1. Test the functionality of the constructed Basic gates using universal gates.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

**VI Relevant Theoretical Background**

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates.

**VII Circuit diagram**

**a) Sample circuit**

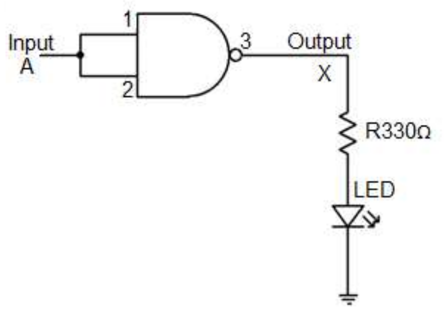


Figure (a)

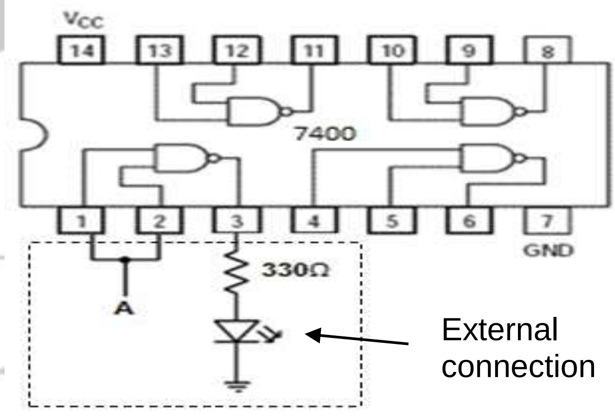


Figure (b)

**Fig. 3.1 NOT gate using NAND gate a) Logic diagram b) IC Circuit diagram**

(Use the appropriate value of the resistor . Diagram shows sample values)

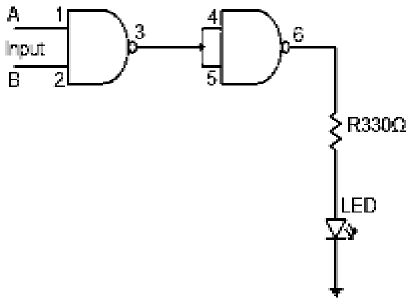


Figure (a)

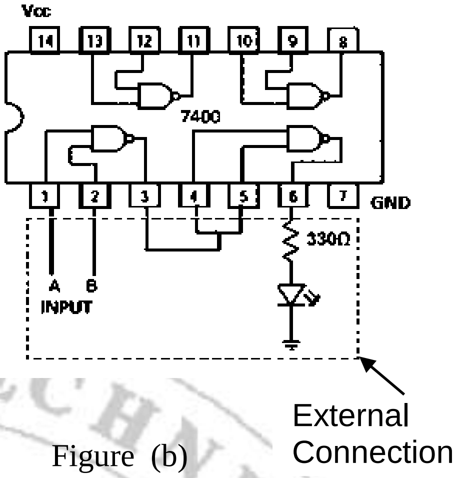


Figure (b)

**Fig. 3.2 AND gate using NAND gate a) Logic diagram b) IC Circuit diagram**

(Use the appropriate value of the resistor . Diagram shows sample values)

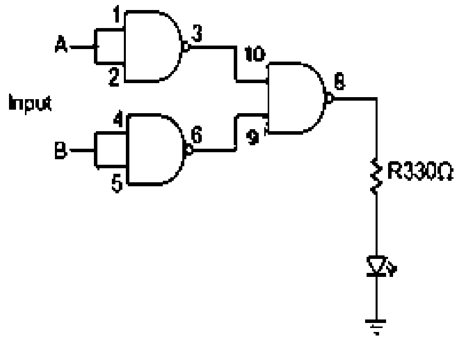


Figure (a)

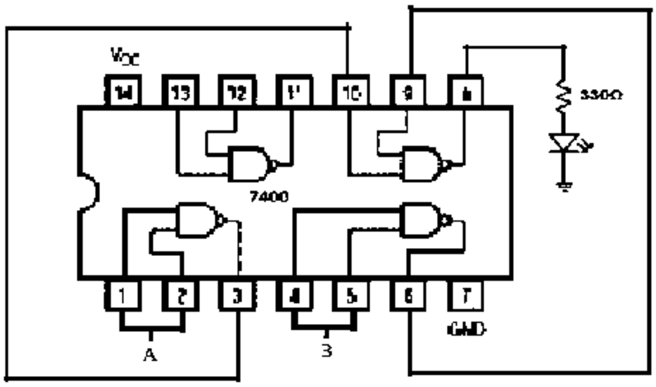


Figure (b)

**Fig. 3.3 OR gate using NAND gate a) Logic diagram b) IC Circuit diagram**

(Use the appropriate value of the resistor . Diagram shows sample values)

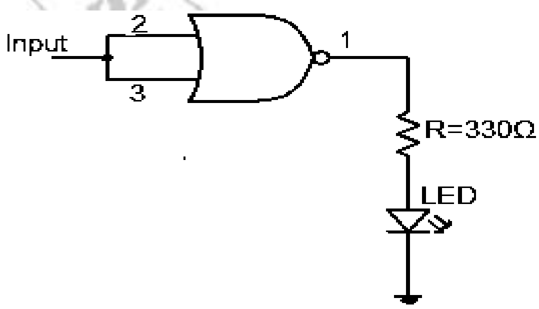


Figure (a)

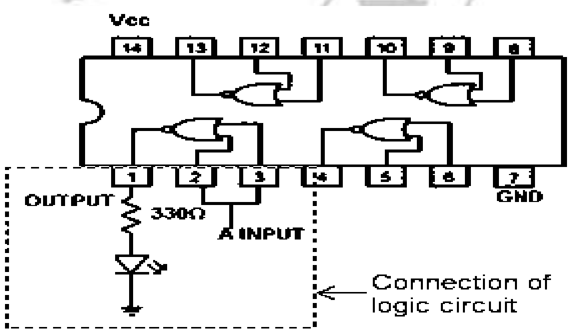


Figure (b)

**Fig. 3.4 NOT gate using NOR gate a) Logic diagram b) IC Circuit diagram**

(Use the appropriate value of the resistor . Diagram shows sample values)

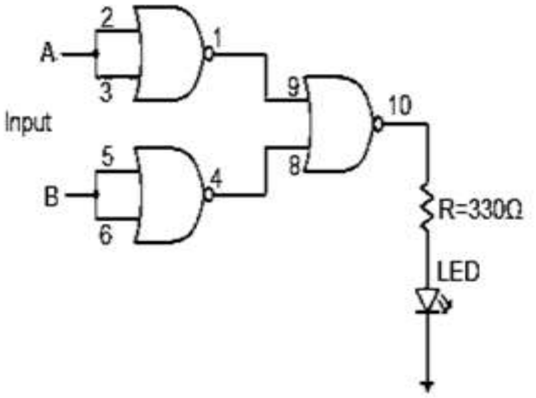


Figure (a)

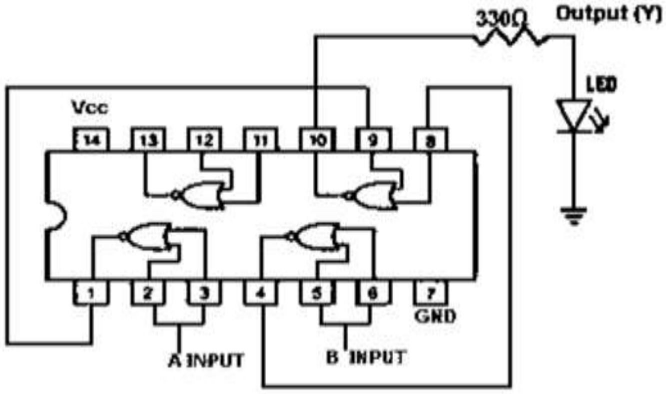


Figure (b)

**Fig.3.5 AND gate using NOR gate a) Logic diagram b) IC Circuit diagram**

(Use the appropriate value of the resistor . Diagram shows sample values)

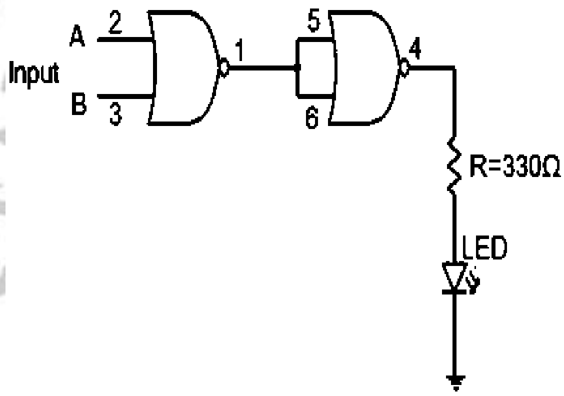


Figure (a)

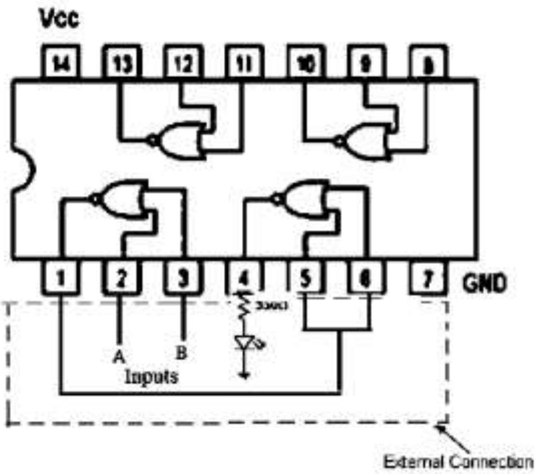


Figure (b)

**Fig. 3.6 OR gate using NOR gate a) Logic diagram b) IC Circuit diagram**

(Use the appropriate value of the resistor . Diagram shows sample values)

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7400, 7402 | 1 Each |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1KΩ/330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Identify pin configuration of logic gate IC 7400 and test with digital IC Tester.
2. Make the connection as shown in figure 3.1-3.3 on breadboard
3. Connect the +5V to Vcc pin of IC and GND pin to ground
4. Observe the LED (on or off) for each combination of input as per truth table
5. Verify the truth table
6. Repeat the process for figure 3.4-3.6.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
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## XII Actual Procedure

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## XIII Observation:

**Table 3.1 a: Observation Table For NOT gate using NAND gate**

| Inputs | NOT | | |
|---|---|---|---|
| A | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) |
| 0(0V) | | | |
| 1(5V) | | | |

**Table 3.1 b: Observation Table For AND, OR gate using NAND gate**

| Inputs | | AND | | | OR | | |
|---|---|---|---|---|---|---|---|
| A | B | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) |
| 0(0V) | 0(0V) | | | | | | |
| 0(0V) | 1(5V) | | | | | | |
| 1(5V) | 0(0V) | | | | | | |
| 1(5V) | 1(5V) | | | | | | |

**Table 3.2 a: Observation Table For NOT gate using NOR gate**

| Inputs | NOT | | |
|---|---|---|---|
| A | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) |
| 0(0V) | | | |
| 1(5V) | | | |

**Table 3.2 b: Observation Table For AND, OR gate using NOR gate**

| Inputs | | AND | | | OR | | |
|---|---|---|---|---|---|---|---|
| A | B | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) |
| 0(0V) | 0(0V) | | | | | | |
| 0(0V) | 1(5V) | | | | | | |
| 1(5V) | 0(0V) | | | | | | |
| 1(5V) | 1(5V) | | | | | | |

**XIV Result(s)**

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**XV Interpretation of results**

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**XVI Conclusion and recommendation**

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**XVII Practical related questions**

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. Design 3 input NOR gate using 2 input NOR gate IC 7402.
2. Draw EX-NOR gate using NAND Gates.
3. Write name of manufacturers of Digital IC 7400, 7402 used in your lab.
4. What is the significance of L, LS and H in the following IC 74L00, 74LS00, and 74H00?

**[Space for Answers]**

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## XVIII References/Suggestions for further reading

1. https://de-iitr.vlabs.ac.in/exp/realization-of-logic-functions/simulation.html
2. https://www.futurlec.com/74/IC7400.shtml
3. https://www.futurlec.com/74/IC7402.shtml

## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| Marks Obtained | | | Dated signature of Teacher |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.4: Construct Exclusive Gates using Universal Gates.**

**I Practical Significance**

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Apply Boolean laws to minimize complex Boolean function.

**IV Laboratory Learning Outcome(s):**

1. Construct Ex-OR, EX- NOR gates using universal gates.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

**VI Relevant Theoretical Background**

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates.

**VII Circuit diagram**

**a) Sample Circuit**

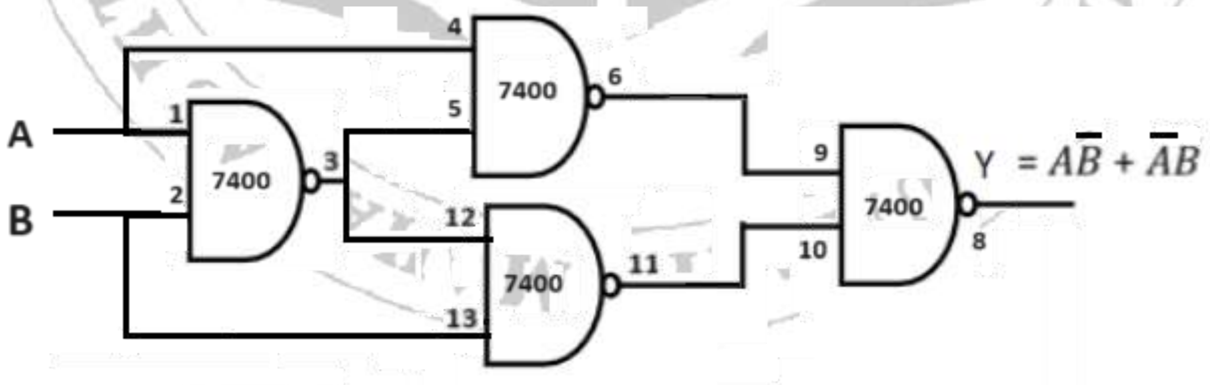


**Fig 4.1: Circuit Diagram : EX-OR gate using NAND gate**

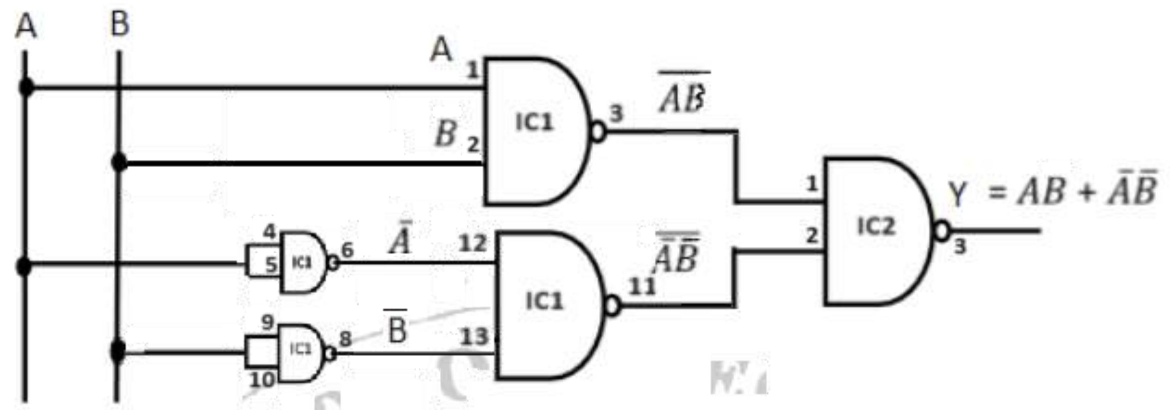


**Fig 4.2: Circuit Diagram: EX-NOR gate using NAND gate**

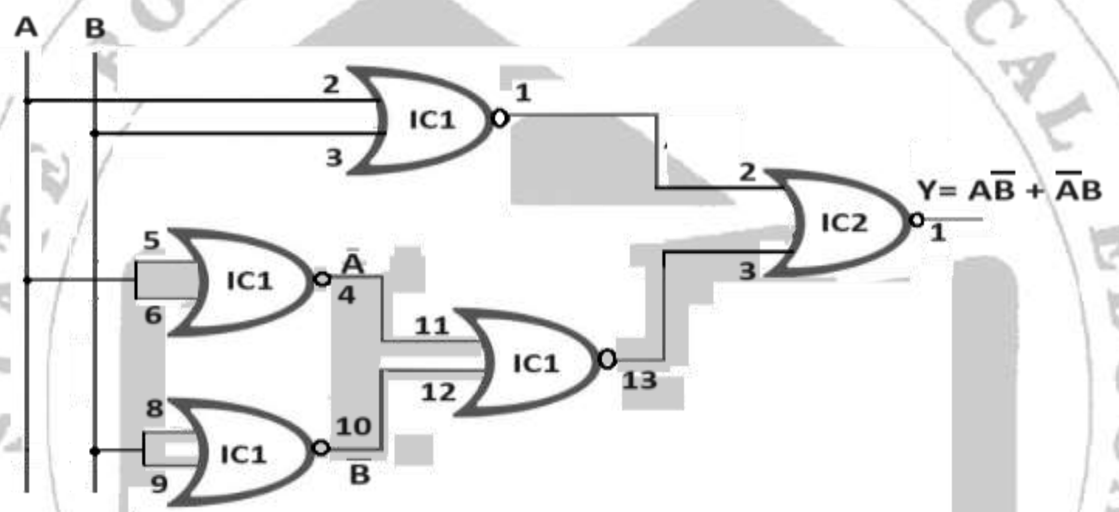


**Fig 4.3: Circuit Diagram : EX-OR gate using NOR gate**

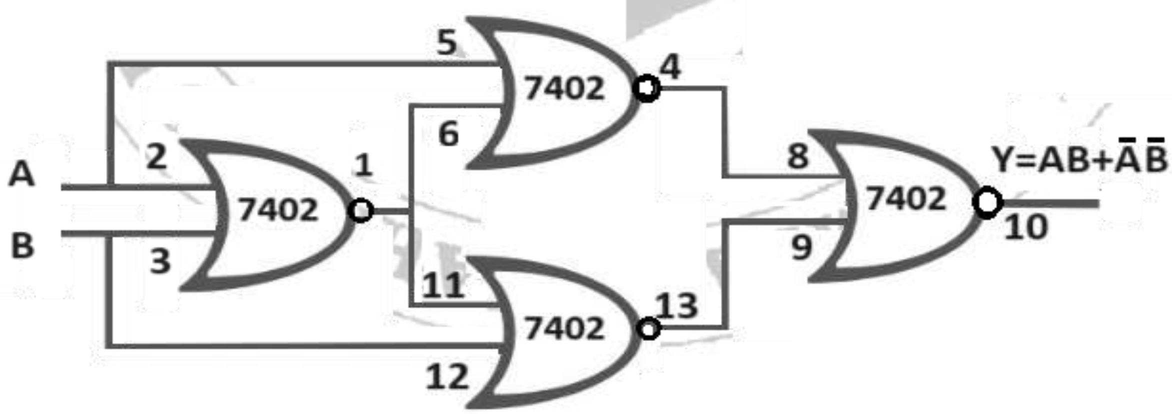


**Fig 4.4: Circuit Diagram: EX-NOR gate using NOR gate**

**b) Actual Circuit**

### VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC’s. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7400, 7402 | 2 Each |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1KΩ/330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Identify pin configuration of logic gate IC 7400 , IC7402 and test with digital IC Tester.
2. Make the connection as shown in figure 4.1-4.2 on breadboard
3. Connect the +5V to +Vcc pin of IC and GND pin to ground
4. Observe the LED (on or off) for each combination of input as per truth table
5. Verify the truth table
6. Repeat the process for figure 4.3-4.4.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
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## XII Actual Procedure

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## XIII Observation:

**Table 4.1: Observation Table For EX-OR & EX-NOR gate using NAND gate**

| Inputs | | EX-OR | | | EX-NOR | | |
|---|---|---|---|---|---|---|---|
| A | B | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) |
| 0(0V) | 0(0V) | | | | | | |
| 0(0V) | 1(5V) | | | | | | |
| 1(5V) | 0(0V) | | | | | | |
| 1(5V) | 1(5V) | | | | | | |

**Table 4.2: Observation Table For EX-OR & EX-NOR gate using NOR gate**

| Inputs | | EX-OR | | | EX-NOR | | |
|---|---|---|---|---|---|---|---|
| A | B | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) | LED Status (ON/OFF) | Logic Level (0/1) | Output voltage (V) |
| 0(0V) | 0(0V) | | | | | | |
| 0(0V) | 1(5V) | | | | | | |
| 1(5V) | 0(0V) | | | | | | |
| 1(5V) | 1(5V) | | | | | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. Write truth table for three input EX-OR & three input EX-NOR gates.
2. Refer diagram 4.1 & measure the voltage of pin 3,6,11.
3. Refer diagram 4.4 & measure the voltage of pin 1,4,13.

**[Space for Answers]**

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## XVIII References/Suggestions for further reading


1. https://de-iitr.vlabs.ac.in/exp/realization-of-logic-functions/simulation.html
2. https://www.futurlec.com/74/IC7400.shtml
3. https://www.futurlec.com/74/IC7402.shtml


## XVIII Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

## Practical No.5: Verify De-Morgan's Theorem (1 and 2).

### I Practical Significance

De Morgan's theorems prove very useful for simplifying Boolean logic expressions because of the way they can 'break' an inversion, which could be the complement of a complex Boolean expression..This practical will enable the students to use De Morgan’s theorem to simplify the complex function for the efficient hardware implementation.

### II Industry/Employer Expected Outcome(s)

Students will be able to test the functionality of the digital circuits/system.

### III Course Level Learning Outcome(s)

Apply Boolean laws to minimize complex Boolean function.

### IV Laboratory Learning Outcome(s):

1. Build the logic circuit on breadboard to verify the De - Morgan's theorems.

### V Relevant Affective Domain related outcome(s)

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

### VI Relevant Theoretical Background

De Morgan’s theorem is used to simplify Boolean expressions and digital circuits.

**De Morgan’s first Theorem:** It states that , the complement of the sum is equal to the product of their individual complements.

The theorem can be expressed by logic equation as

$$\overline{\boldsymbol{A}+\boldsymbol{B}} = \overline{\boldsymbol{A}}\ .\ \overline{\boldsymbol{B}}$$

NOR gate = Bubbled AND gate

**De Morgan’s second Theorem:** It states that , the complement of a product is equal to the sum of their individual complements.

The theorem can be expressed by logic equation as

$$\overline{\boldsymbol{A}.\boldsymbol{B}} = = \overline{\boldsymbol{A}} + \overline{\boldsymbol{B}}$$

NAND gate = Bubbled OR gate

## VII Circuit diagram

### a) Sample Circuit

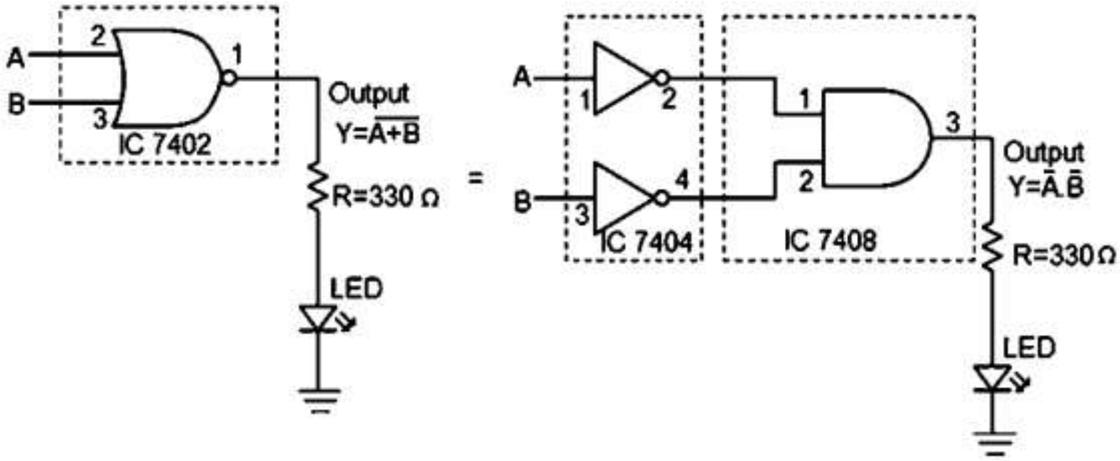


**Fig 5.1: De Morgan's first theorem**

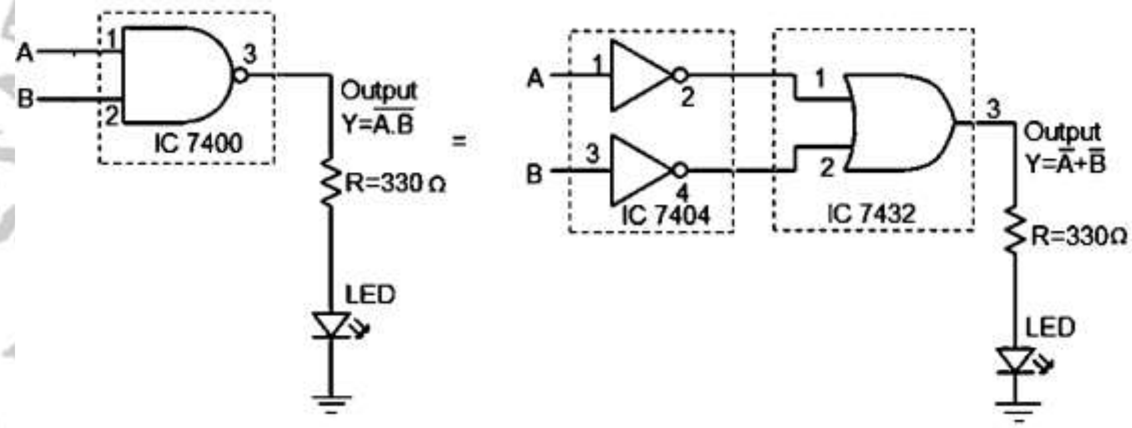


**Fig 5.2: De Morgan's second theorem**

### b) Actual Circuit

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC’s. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7400, 7404,7432,7402,7408. | 1 Each |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1KΩ/330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Identify pin configuration of logic gate IC’s and test with digital IC Tester.
2. Mount the IC’s on the breadboard
3. Make the connection as per fig 5.1for LHS as well as RHS side and give supply voltage to the relevant pin as per logic level.
4. Observe the LED (on or off) for each combination of input as per truth table
5. Verify the truth table
6. Repeat the process for figure 5.2.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |

## XII Actual Procedure

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## XIII Observation:

**Table 5.1: Observation Table: De Morgan's first theorem**

| **Inputs** | | **Outputs** | |
|---|---|---|---|
| **A** | **B** | **LHS=** $\overline{\boldsymbol{A}+\boldsymbol{B}}$ | **RHS=** $\overline{\boldsymbol{A}}\ .\ \overline{\boldsymbol{B}}$ |
| 0 | 0 | | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

**Table 5.2: Observation Table: De Morgan's second theorem**

| **Inputs** | | **Outputs** | |
|---|---|---|---|
| **A** | **B** | **LHS=** $\overline{\boldsymbol{A}.\boldsymbol{B}}$ | **RHS=** $\overline{\boldsymbol{A}}+\overline{\boldsymbol{B}}$ |
| 0 | 0 | | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. List the IC numbers used in De Morgan's first theorem.
2. List the IC numbers used in De Morgan's second theorem.
3. Simplify the expression: $Y=\overline{\overline{(A+B)}\,\overline{\overline{[C\,\overline{(A+B)}]}}}$

**[Space for Answers]**

## XVIII References/Suggestions for further reading


1. https://www.futurlec.com/74/IC7404.shtml
2. https://www.electroschematics.com/wp-content/uploads/2013/07/7408-datasheet.pdf
3. https://www.ti.com/lit/ds/symlink/sn5432.pdf?ts=1720330546912&ref_url=https%253A%252F%252Fwww.google.com%252F
4. https://www.futurlec.com/74/IC7400.shtml
5. https://www.futurlec.com/74/IC7402.shtml
6. https://www.youtube.com/watch?v=I8WdCozPTeQ


## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| Marks Obtained | | | Dated signature of Teacher |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.6: Implement 2 input, 3 input Adder Circuit.**

**I Practical Significance**

In many computers and other kinds of processors, adders are used in the arithmetic logic units (ALUs). They are also used in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators and similar operations.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop combinational logic circuits for given applications.

**IV Laboratory Learning Outcome(s):**

1. Verify the truth table of Half and Full adder circuits for the given input.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

**VI Relevant Theoretical Background**

A half adder is a digital logic circuit that performs binary addition of two single-bit binary numbers. It has two inputs, A and B, and two outputs, SUM(S) and CARRY (C). The SUM output is the least significant bit (LSB) of the result, while the CARRY output is the most significant bit (MSB) of the result, indicating whether there was a carry-over from the addition of the two inputs. The half adder can be implemented using one EX-OR gate and one AND gate. The C output is 1 only when both inputs are 1.

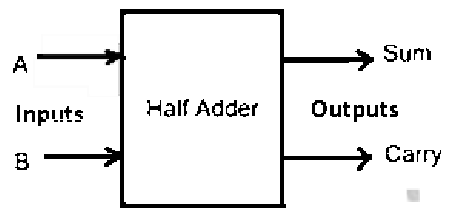


**Fig 6.1:Block Diagram of Half adder**

The full adder is a combinational circuit which is used to perform addition of three input bits. The full adder adds the bits A and B and the carry from the previous bits addition called the carry in (Cin) and the outputs the sum bit (S) and the carry bit called the carry out (Cout). The variable S gives the value of the least significant bit of the sum. The variable Cout gives the output carry.

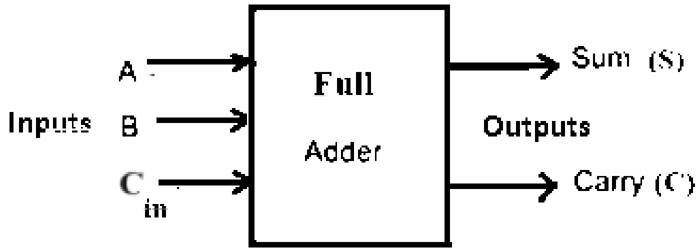


**Fig 6.2: Block Diagram of Full adder**

**VII Circuit diagram**

**a) Sample circuit**

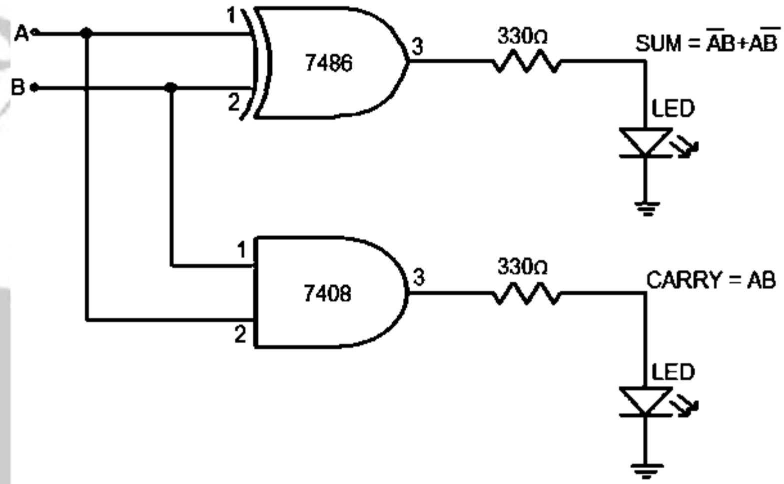


**Fig 6.3: Half adder Circuit Diagram**

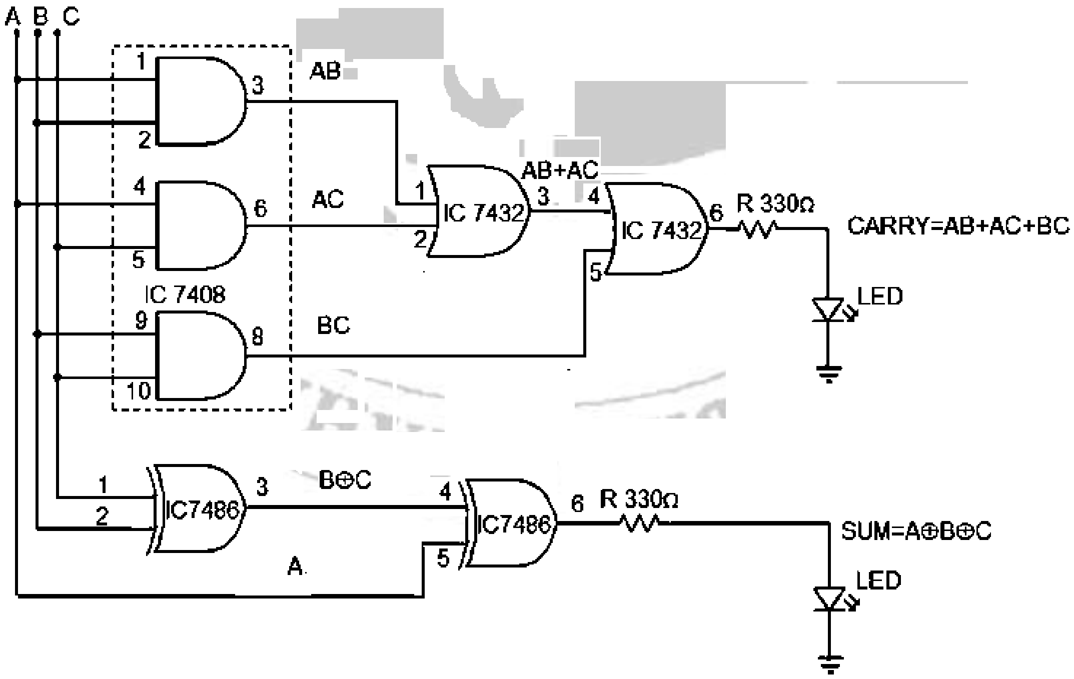


**Fig 6.4: Full adder Circuit Diagram**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7486, 7408,7432. | 1 Each |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1KΩ/330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Test the IC using Digital IC tester
2. Mount the IC on the breadboard and Make the connection as per figure 6.3.
3. Connect the +5V to +Vcc pin of IC and GND pin to ground
4. Observe the LED (on or off) for each combination of input as per truth table
5. Verify the truth table
6. Repeat the procedure for figure 6.4.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure

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## XIII Observation:

**Table 6.1: Observation Table for Half Adder**

| Inputs | | Output | | | |
|---|---|---|---|---|---|
| | | Sum | | Carry | |
| A | B | Logic Level (1/0) | Output voltage (v) | Logic Level (1/0) | Output voltage (v) |
| 0 (0V) | 0(0V) | | | | |
| 0(0V) | 1(5V) | | | | |
| 1(5V) | 0(0V) | | | | |
| 1(5V) | 1(5V) | | | | |

**Table 6.2: Observation Table for Full Adder**

| Inputs | | | Output | | | |
|---|---|---|---|---|---|---|
| | | | Sum | | Carry | |
| A | B | C | Logic Level (1/0) | Output voltage (v) | Logic Level (1/0) | Output voltage (v) |
| 0 (0V) | 0(0V) | 0(0V) | | | | |
| 0(0V) | 0(0V) | 1(5V) | | | | |
| 0(0V) | 1(5V) | 0(0V) | | | | |
| 0(0V) | 1(5V) | 1(5V) | | | | |
| 1(5V) | 0(0V) | 0(0V) | | | | |
| 1(5V) | 0(0V) | 1(5V) | | | | |
| 1(5V) | 1(5V) | 0(0V) | | | | |
| 1(5V) | 1(5V) | 1(5V) | | | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. State drawback of Half Adder circuit.
2. Draw half adder using NAND gates only.
3. Design Half Adder using K-map.
4. Draw Full adder circuit using Half adder circuits.

**[Space for Answers]**

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## XVIII References/Suggestions for further reading


1. https://de-iitr.vlabs.ac.in/exp/half-full-adder/index.html
2. https://www.futurlec.com/74/IC7402.shtml
3. https://www.ntchip.com/electronics-news/ic-7486-chip
4. https://www.ti.com/lit/ds/symlink/sn5432.pdf?ts=1720330546912&ref_url=https%253A%252F%252Fwww.google.com%252F


## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | 60 % |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| Marks Obtained | | | Dated signature of Teacher |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

## Practical No.7: Implement 2 input, 3 input Subtractor Circuit.

**I Practical Significance**

Subtractor is used in systems where subtraction operations are required, such as in arithmetic units of microprocessors, calculators, digital signal processing circuits, and other digital systems where subtraction is needed.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop combinational logic circuits for given applications.

**IV Laboratory Learning Outcome(s):**

1. Verify the truth table of Half and Full subtractor using Boolean expressions.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

**VI Relevant Theoretical Background**

A half subtractor is a combinational circuit used in digital electronics for subtracting two single-bit binary numbers. It has two inputs - minuend (A) and subtrahend (B) - and two outputs - the difference (D) and the Borrow (B).It is made of EX-OR gate, NOT gate (Inverter), and AND gate. The B output is 1 only when the subtrahend (B) is greater than the minuend (A).

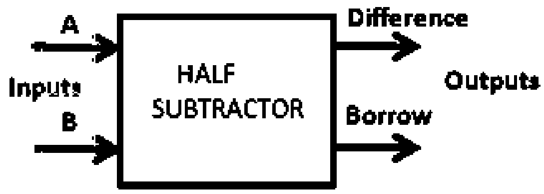


**Fig 7.1: Block diagram of Half subtractor**

Full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend. In full subtractor ‘1’ is borrowed by the previous adjacent lower minuend bit. Hence these three bits are considered at the input of a full subtractor. There are two outputs that are DIFFERENCE (D) and BORROW ( Bo).

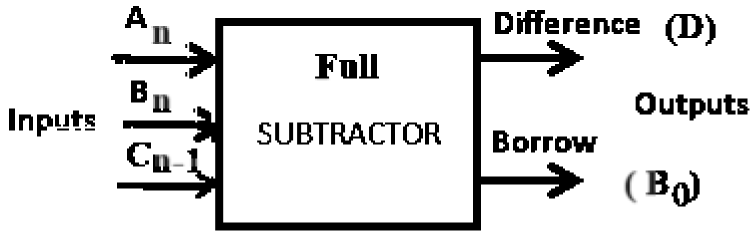


**Fig 7.2: Block diagram of Full subtractor**

**VII Circuit diagram**

**a) Sample circuit**

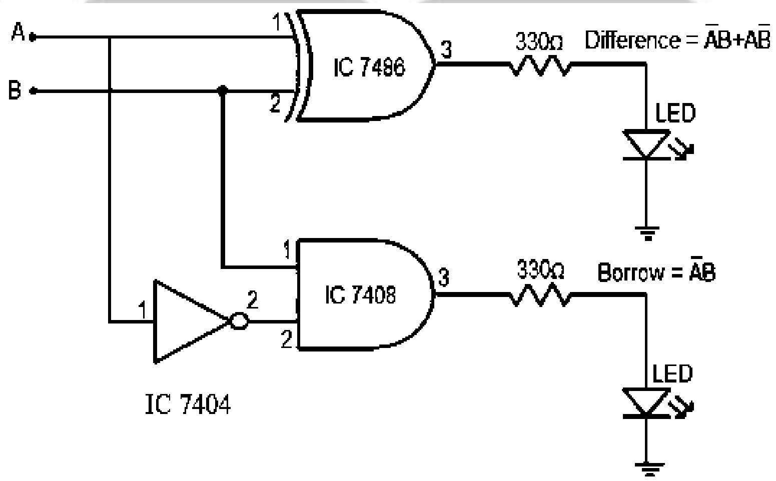


**Fig 7.3:Half subtractor Circuit Diagram**

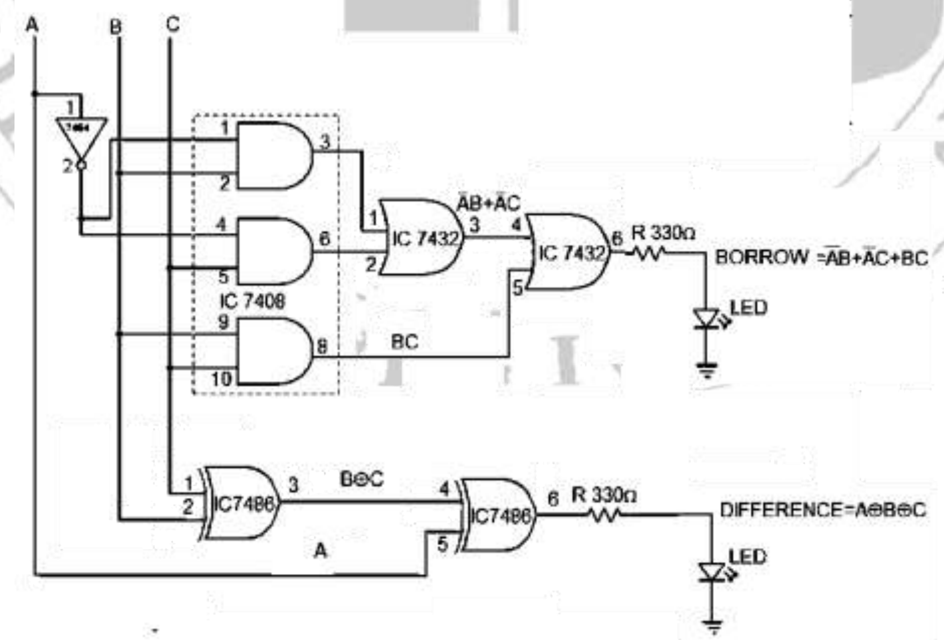


**Fig 7.4:Full subtractor Circuit Diagram**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7486, 7404,7408.7432 | 1 Each |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1KΩ/330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Test the IC using Digital IC tester
2. Mount the IC on the breadboard
3. Make the connection as per figure 7.3.
4. Connect the +5V to +Vcc pin of IC and GND pin to ground
5. Observe the LED (on or off) for each combination of input as per truth table
6. Verify the truth table
7. Repeat the procedure for figure.7.4.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
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## XII Actual Procedure

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## XIII Observation:

**Table 7.1: Observation Table For Half Subtractor**

| Inputs | | Output | | | |
|---|---|---|---|---|---|
| | | Difference | | Borrow | |
| A | B | Logic Level (1/0) | Output voltage (v) | Logic Level (1/0) | Output voltage (v) |
| 0 (0V) | 0(0V) | | | | |
| 0(0V) | 1(5V) | | | | |
| 1(5V) | 0(0V) | | | | |
| 1(5V) | 1(5V) | | | | |

**Table 7.2: Observation Table For Full Subtractor**

| Inputs | | | Output | | | |
|---|---|---|---|---|---|---|
| | | | Difference | | Borrow | |
| A | B | C | Logic Level (1/0) | Output voltage (v) | Logic Level (1/0) | Output voltage (v) |
| 0 (0V) | 0(0V) | 0(0V) | | | | |
| 0(0V) | 0(0V) | 1(5V) | | | | |
| 0(0V) | 1(5V) | 0(0V) | | | | |
| 0(0V) | 1(5V) | 1(5V) | | | | |
| 1(5V) | 0(0V) | 0(0V) | | | | |
| 1(5V) | 0(0V) | 1(5V) | | | | |
| 1(5V) | 1(5V) | 0(0V) | | | | |
| 1(5V) | 1(5V) | 1(5V) | | | | |

**XIV Result(s)**

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**XV Interpretation of results**

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**XVI Conclusion and recommendation**

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**XVII Practical related questions**

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. Draw half subtractor using NAND gates only.
2. Design Half subtractor using K-map.
3. Draw a full subtractor using half subtractor circuits.

**[Space for Answers]**

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## XVIII References/Suggestions for further reading


1. https://de-iitr.vlabs.ac.in/exp/half-full-subtractor/index.html
2. https://www.futurlec.com/74/IC7402.shtml
3. https://www.ntchip.com/electronics-news/ic-7486-chip
4. https://www.ti.com/lit/ds/symlink/sn5432.pdf?ts=1720330546912&ref_url=https%253A%252F%252Fwww.google.com%252F
5. https://www.futurlec.com/74/IC7404.shtml


## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.8: Test the output of BCD to 7 Segment Decoder using Digital IC for the given inputs.**

**I Practical Significance**

BCD is an abbreviation for binary-coded decimal. BCD is a way of representing decimal numbers in binary form. The IC takes a 4-bit BCD input and converts it into the corresponding 7-segment display outputs. It is used to display decimal numbers.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop combinational logic circuits for given applications.

**IV Laboratory Learning Outcome(s):**

1. Construct and test BCD to 7 segment using Digital IC.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions.

**VI Relevant Theoretical Background**

A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of 2n unique output lines. The IC7447 is a BCD to 7-segment pattern converter. The IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs the relevant 7 segment code. A seven segment decoder is an IC decoder that can be used to drive a seven segment indicator. There are two types of 7-segment digital display 1. Common anode display (CAD) and 2.common cathode display (CCD). Each decoder driver has 4 BCD inputs and 7 output pins (a to g segment).

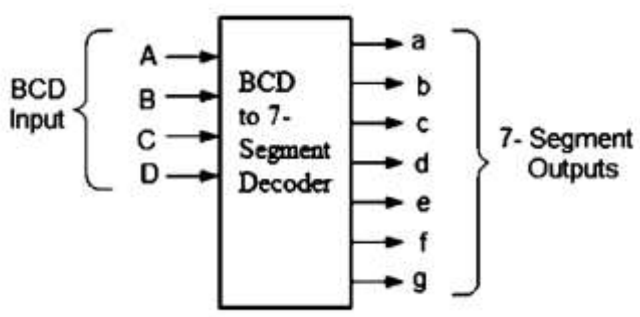



**Fig. 8.1 BCD to 7-Segment Decoder**

**Common Cathode Display (CCD):**

Common cathode has all the cathodes of the 7-segments connected directly together to ground (Logic 0).The individual segments are illuminated by application of high (Logic1) signal to the individual anode terminals. For common cathode LED displays the ICs are IC 7448, IC 74248,IC 7449 etc. are used.

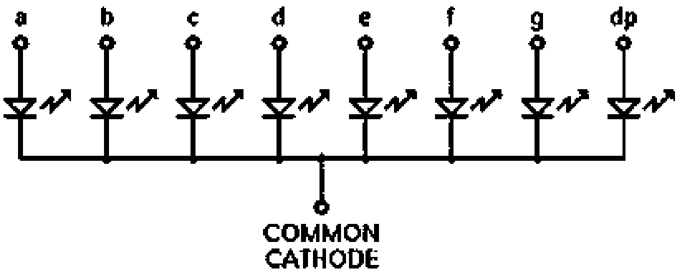



**Fig. 8.2 Common Cathode Display (CCD)**

**Common Anode Display (CAD):**

Common anode has all the anodes of the 7-segments connected together to VCC (Logic 1).The individual segments are illuminated by connecting the individual cathode terminals to low (Logic0) signals to the individual cathode terminals. For common anode LED displays the ICs are IC 7446, IC 74246, IC 7447 etc. are used.

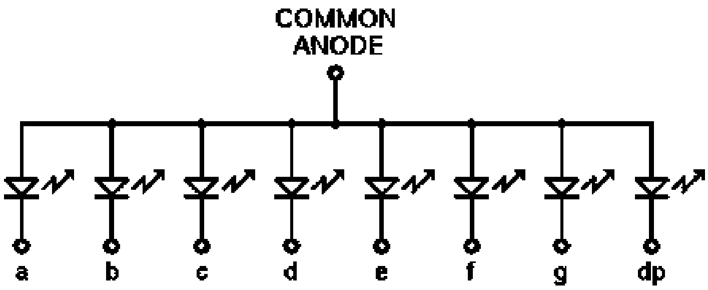
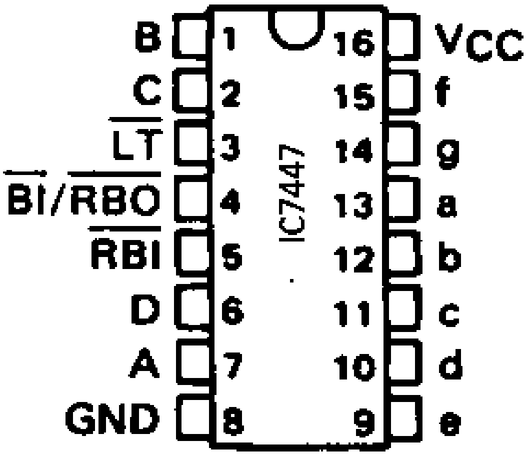



**Fig. 8.3 Common Anode Display (CAD)**

Courtesy:(https://arduino.stackexchange.com/questions/16858/leds-difference-between-common-anode-and-common-cathode)

**IC 7447(BCD to 7-Segment decoder IC)**

IC 7447 is BCD to 7-Segment decoder IC whose output is active low depending on the corresponding BCD inputs so it is used to drive common anode 7- segment displays.




| Pin Name | Description |
|---|---|
| D,C,B,A | BCD inputs |
| a to g | Outputs |
| $\overline{LT}$ | Lamp Test |
| $\overline{RBI}$ | Ripple Blanking Input |
| $\overline{BI}$ | Blanking Input |
| $\overline{RBO}$ | Ripple Blanking Output |

**Fig. 8.4 IC 7447 pin diagram**

**IC 7448(BCD to 7-Segment decoder IC)**

IC 7448 is BCD to 7-Segment decoder IC whose output is active high depending on the corresponding BCD inputs so it is used to drive common cathode 7- segment displays

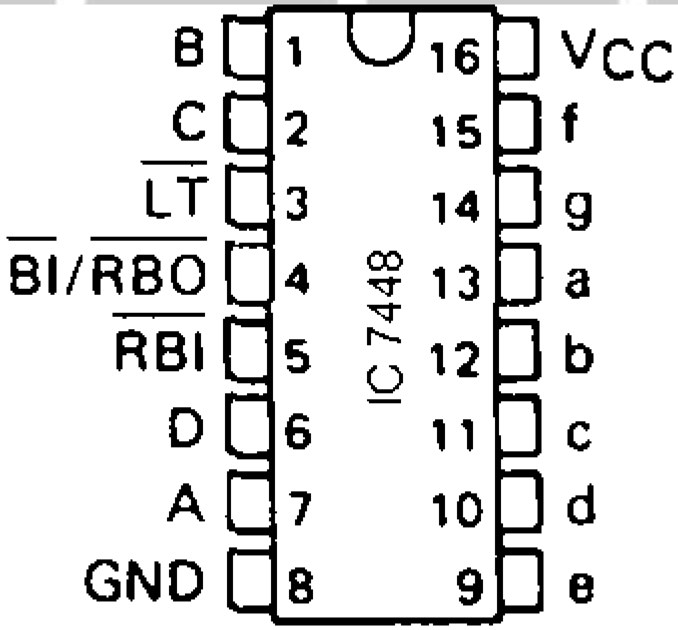
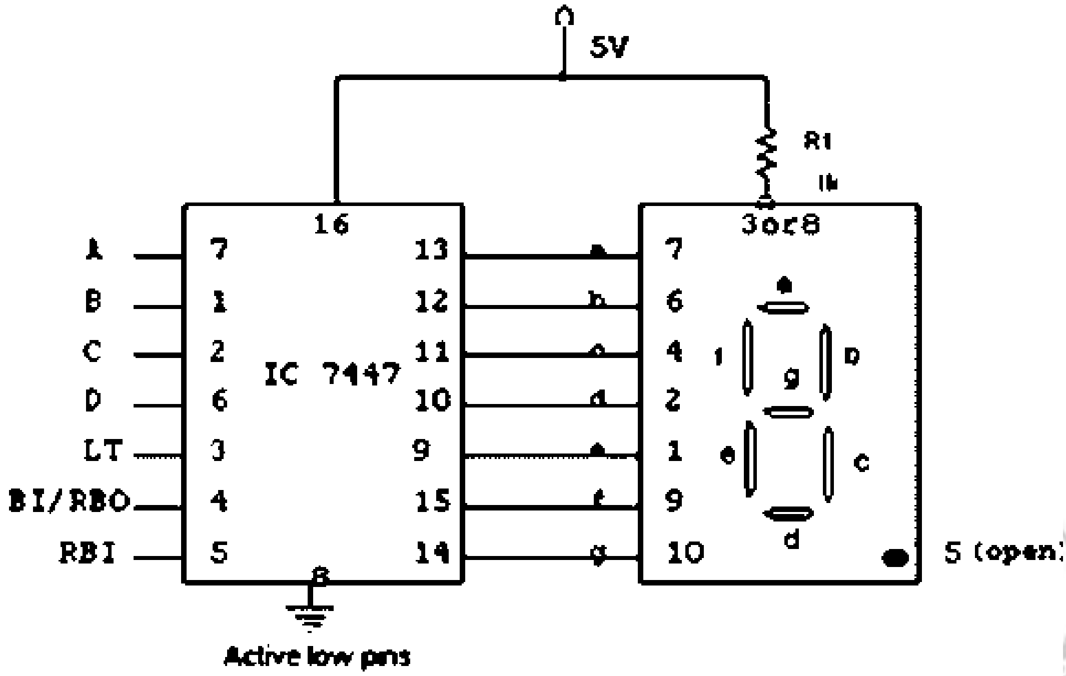



**Fig. 8.5 IC 7448 pin diagram**

## VII Circuit diagram

### a) Sample Circuit




**For normal functioning of IC 7447 Pin number 3, 4, 5 should be connected to logic 1Vcc**

Courtesy: (http://www.bragitoff.com/2015/10/bcd-to-7-segment-decoderdriver/)

**Fig 8.6: Circuit Diagram**

### b) Actual circuit

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC’s. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7447 or 7448 | 1 Each |
| 6 | Common anode 7-seg Display | IC FND 507/LT 542 | 1 |
| 7 | Common cathode 7-seg Display | IC LT 543 | 1 |
| 8 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 9 | Resistor | 1KΩ/330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Test the IC using Digital IC tester
2. Make the connection as per fig 8.6
3. Connect different BCD inputs from 0000 to 1001 and note down the corresponding output on the display.
4. Observe the outputs on a 7- segment display.
5. Connect the +5V to +Vcc pin of IC and GND pin to ground
6. Observe the LED (on or off) for each combination of input as per truth table
7. Verify the truth table

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
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## XII Actual Procedure

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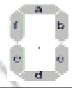
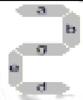
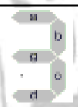
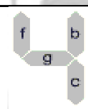
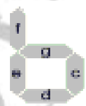
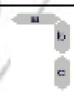
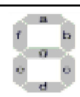
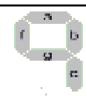
## XIII Observation:

**Table 8.1: Observation Table common anode display**

| BCD Inputs | | | | 7-Segment Coded Output | | | | | | | Display output |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | a | b | c | d | e | f | g | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |  |
| 0 | 0 | 1 | 0 | | | | | | | |  |
| 0 | 0 | 1 | 1 | | | | | | | |  |
| 0 | 1 | 0 | 0 | | | | | | | |  |
| 0 | 1 | 0 | 1 | | | | | | | |  |
| 0 | 1 | 1 | 0 | | | | | | | |  |
| 0 | 1 | 1 | 1 | | | | | | | |  |
| 1 | 0 | 0 | 0 | | | | | | | |  |
| 1 | 0 | 0 | 1 | | | | | | | |  |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. Write down the output for the 7-segment decoder using a common cathode display .
2. Write the functions of pin No. 3, 4, and 5 of IC 7448.
3. List different types of decoder.

**[Space for Answers]**

Ans 1 : output for the 7-segment decoder using a common cathode display

| BCD Inputs | | | | 7-Segment Coded Output | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **D** | **C** | **B** | **A** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| **0** | **0** | **0** | **0** | | | | | | | |
| **0** | **0** | **0** | **1** | | | | | | | |
| **0** | **0** | **1** | **0** | | | | | | | |
| **0** | **0** | **1** | **1** | | | | | | | |
| **0** | **1** | **0** | **0** | | | | | | | |
| **0** | **1** | **0** | **1** | | | | | | | |
| **0** | **1** | **1** | **0** | | | | | | | |
| **0** | **1** | **1** | **1** | | | | | | | |
| **1** | **0** | **0** | **0** | | | | | | | |
| **1** | **0** | **0** | **1** | | | | | | | |

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## XVIII References/Suggestions for further reading


1. https://dec-iitkgp.vlabs.ac.in/exp/7-segment-led-display/simulation.html
2. https://dec-iitkgp.vlabs.ac.in/exp/7-segment-led-display/index.html
3. https://de-iitg.vlabs.ac.in/exp/bcd-to-led/theory.html
4. https://www.electroschematics.com/wp-content/uploads/2013/01/7447-datasheet.pdf


## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.9: Check the output of comparator circuit consists of Digital IC.**

**I Practical Significance**

As data comparison is mostly required in many digital systems at the time of logical or arithmetic functions, digital comparators are the one best option to compare data. Digital comparators are the most appropriate combinational logic circuits used to compare relative magnitudes of two binary numbers.A comparator is a decision-making tool and it holds the ability to be executed in numerous
control devices.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop combinational logic circuits for given applications.

**IV Laboratory Learning Outcome(s):**

1. Build/Test 2 or 4 bit Magnitude comparator using Digital IC.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the components and equipment carefully.
Follow all safety precautions**.**

**VI Relevant Theoretical Background**

A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than, or greater than the other binary number.

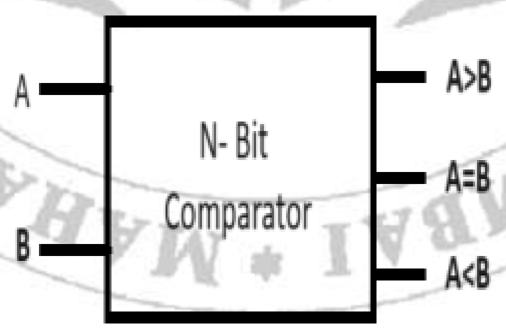


**Fig.9.1 Comparator block diagram**

Circuit have two inputs one for A and the other for B and have three output terminals, one for A > B condition, one for A = B condition, and one for A < B condition.

## VII Circuit diagram

### a) Sample circuit

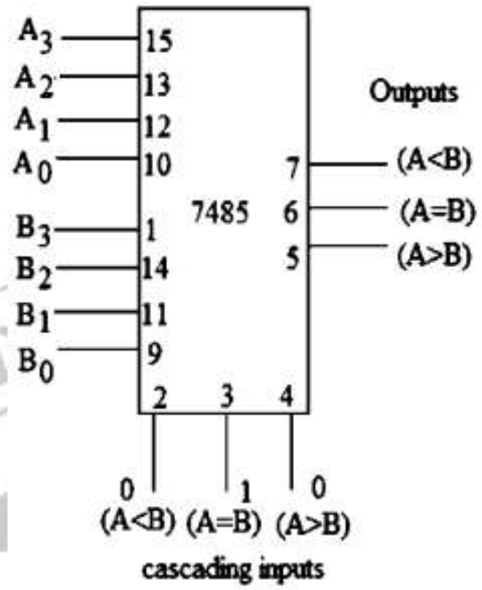


**Fig 9.2: Circuit Diagram : 4 bit magnitude comparator**

### b) Actual circuit

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | Digital Multimeter: 3 1/2 digit display. | 2 |
| 2 | Digital IC Tester | Tests a wide range of Digital IC's such as 74 Series, 40/45 Series of CMOS IC's. | 1 |
| 3 | DC power supply | +5 V Fixed power supply | 1 |
| 4 | Breadboard | 5.5cm X 17 cm | 1 |
| 5 | IC | 7485 | 1 |
| 6 | LED | Red /Yellow color 5 mm | 1 |
| 7 | Connecting wires | Single strand 0.6 mm Teflon coating | As required |
| 8 | Resistor | 1KΩ/330Ω | As required |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Test the IC using Digital IC tester
2. Mount the IC on the breadboard
3. Make the connection as per fig 9.2.
4. Connect the +5V to +Vcc pin of IC and GND pin to ground
5. Observe the LED (on or off) for given combination of input as per truth table
6. Verify the truth table

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
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## XII Actual Procedure

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## XIII Observation:

**Table 9.1: Observation Table**

| Input A | | | | Input B | | | | Output | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_3$ | $A_2$ | $A_1$ | $A_0$ | $B_3$ | $B_2$ | $B_1$ | $B_o$ | A<B | A=B | A>B |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | | | |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
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(Few sample input combinations are given above as 256 combinations of inputs are possible . Teacher can add 4 extra combinations for practice)

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. Draw logic circuit for 1 bit magnitude comparator also write its truth table
2. Draw pin diagram of IC 7485 also write its truth table.
3. List the name manufacture of IC 7485 & list any four electrical characteristics of it.

**[Space for Answers]**

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**XVIII References/Suggestions for further reading**

1. https://dld-iitb.vlabs.ac.in/exp/four-bit-digital-comparator/index.html
2. https://www.nteinc.com/specs/7400to7499/pdf/nte7485.pdf

**XIX Assessment Scheme**

| Performance Indicators | | Weightage |
|---|---|---|
| **Process Related : 15 Marks** | | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| **Product Related: 10 Marks** | | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| **Total ( 25 Marks)** | | **100 %** |

| Marks Obtained | | | Dated signature of Teacher |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.10: Build and test the functionality of 4:1/8:1 Multiplexer.**

## I Practical Significance

In most of the electronic systems, the digital data is available on more than one line. It is necessary to route this data over a single line. Under such circumstances we require a circuit which selects one of the many inputs at a time. This circuit is a multiplexer, which has many inputs, one output and some select line inputs. Practical significance lies in their ability to simplify complex digital designs, reduce hardware complexity, and improve system performance

## II Industry/Employer Expected Outcome(s)

Students will be able to test the functionality of the digital circuits/system.

## III Course Level Learning Outcome(s)

Develop combinational logic circuits for given applications.

## IV Laboratory Learning Outcome(s):

1. Build/Test function of MUX Digital IC

## V Relevant Affective Domain related outcome(s)

Significance of select lines to select one output from many inputs.
Handle the component and equipment carefully.
Follow all safety precaution

## VI Relevant Theoretical Background

Multiplexer is a combinational circuit that is one of the most widely used in digital design. The multiplexer is a data selector which gets one out of several inputs to a single output. It has n data inputs and one output line and m select lines where $2^m = n$ shown in fig10.1. Depending upon the digital inputs applied at the select inputs one out of n data input is selected and transmitted to a single output channel. Normally strobe (E) input is incorporated which is generally active low which enables the multiplexer when it is LOW. Strobe input helps in cascading. IC 74l5lA is an 8: 1 multiplexer which provides two complementary outputs Y and $\underline{Y}$ The output Y is same as the selected input and $\underline{Y}$ is its complement. The n: 1 multiplexer can be used to realize m variable function. ($2^m$= n, m is no. of select inputs)

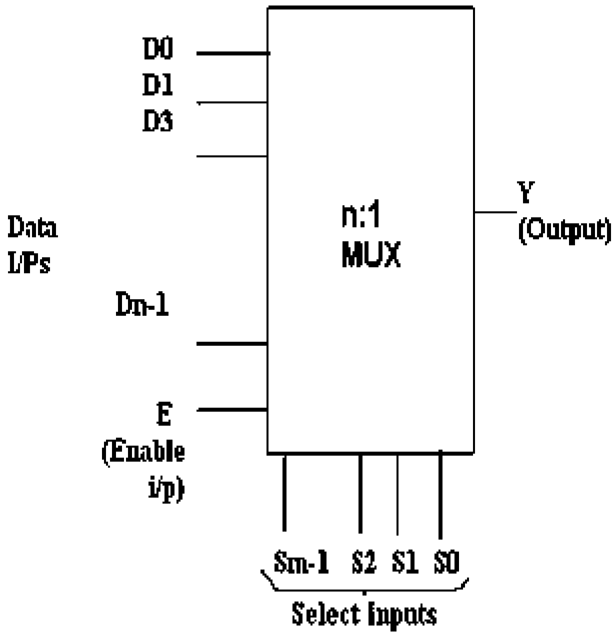



**Fig 10.1: Block diagram of n: 1 Multiplexer**

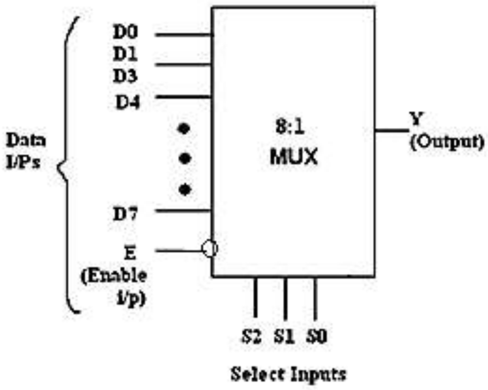
Curtesy:https://www.google.co.in/search?client=firefox-b&biw=1366&bih=654&tbm=isc

**Types of Multiplexer (MUX):**

1. 2:1 MUX (2 lines to 1 line)
2. 4:1 MUX (4 lines to 1 line)
3. 8:1 MUX (8 lines to 1 line)
4. 16:1 MUX (16 lines to 1 line)

**List of ICs which provides multiplexing**

| IC No. | Function | Output State |
|---|---|---|
| 74157 | Quad 2:1 MUX | Output same as input given |
| 74158 | Quad 2:1 MUX | Output is inverted input |
| 74153 | Dual 4:1 MUX | Output same as input |
| 74352 | Dual 4:1 MUX | Output is inverted input |
| 74151A | 8:1 MUX | Both outputs available (i.e. complementary outputs) |
| 74151 | 8:1 MUX | Output is inverted input |
| 74150 | 16:1 MUX | Output is inverted input |




| Enable | Select Inputs | | | Output |
|---|---|---|---|---|
| E | S2 | S1 | S0 | Y |
| 1 | X | X | X | 0 |
| 0 | 0 | 0 | 0 | D0 |
| 0 | 0 | 0 | 1 | D1 |
| 0 | 0 | 1 | 0 | D2 |
| 0 | 0 | 1 | 1 | D3 |
| 0 | 0 | 0 | 0 | D4 |
| 0 | 0 | 0 | 1 | D5 |
| 0 | 0 | 1 | 0 | D6 |
| 0 | 0 | 1 | 1 | D7 |

**(E=1 for active high E=0 for active low)**

**Fig 10.2: Block diagram of 8: 1 MUX, Truth Table of 8:1 MUX**

## VII Circuit diagram

### a) Sample circuit

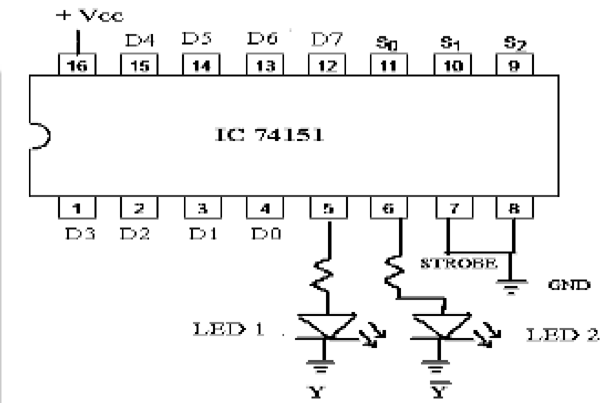



**Fig 10.3: Circuit Diagram (8:1 Mux IC)**

### b) Actual circuit

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | 74151/74150 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 4(3 for Select Lines and One for outputs) |
| 8 | Resistor | 220Ω/330Ω | 2 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Test the IC using Digital IC tester
2. Mount the IC on the breadboard
3. Make the connection as per fig 10.3
4. Connect the +5V to +Vcc pin of IC and GND pin to ground
5. Observe the LED (on or off) for each combination of input as per truth table
6. Verify the truth table

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
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## XII Actual Procedure

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## XIII Observation:

**Table 10.1: Observation Table**

<table>
<tr><th colspan="5">Inputs</th><th colspan="2">Outputs</th><th colspan="2">Outputs</th></tr>
<tr><th>Strobe</th><th>Data Input</th><th colspan="3">Select Input</th><th rowspan="2">Y</th><th rowspan="2">$\overline{Y}$</th><th rowspan="2">Y<br>(O/P volt)</th><th rowspan="2">$\overline{Y}$<br>(O/P volt)</th></tr>
<tr><th>G</th><th>$D_n$</th><th>$S_2$</th><th>$S_1$</th><th>$S_0$</th></tr>
<tr><td>0</td><td rowspan="9">$D_0$=0<br>$D_1$=1<br>$D_2$=1<br>$D_3$=0<br>$D_4$=0<br>$D_5$=1<br>$D_6$=1<br>$D_7$=0</td><td>0 (0V)</td><td>0 (0V)</td><td>0 (0V)</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>0 (0V)</td><td>0 (0V)</td><td>1 (5V)</td><td></td><td></td><td></td><td></td></tr>
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<tr><td>1</td><td>X</td><td>X</td><td>X</td><td></td><td></td><td></td><td></td></tr>
</table>

**(Write the observation with respect to Inputs)**

(Note: ‘X’ indicates the don’t care condition. It means the status of selected input may be any combination)

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are a few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.**

1. List the function of the Strobe (G) pin?
2. List the absolute maximum ratings of IC 74151.
3. List the name of manufacturers of ICS used for this practicals?
4. List the applications where MUX is used?

**[Space for Answers]**

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**XVIII References/Suggestions for further reading**


1. https://datasheetspdf.com/datasheet/74151.html
2. https://dec-iitkgp.vlabs.ac.in/exp/functions-using-multiplexers/(Virtual Lab Link)
3. https://www.youtube.com/watch?v=JR6_a3KPKHE (NPTEL Video Link on Multiplexer)


**XIX Assessment Scheme**

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.11: Build and test the functionality of 1:4/1:8 Demultiplexer.**

## I Practical Significance

A demultiplexer (or demux) is a electronic circuit or device which has single input ,n outputs and m number select lines. The input line is connected to any one output line depending upon the select lines input logic. An electronic demultiplexer can be considered as a single-input, multiple-output switch.Demultiplexers are mainly used in Boolean function generators and decoder circuits.

## II Industry/Employer Expected Outcome(s)

Students will be able to test the functionality of the digital circuits/system.

## III Course Level Learning Outcome(s)

Develop combinational logic circuits for given applications.

## IV Laboratory Learning Outcome(s):

1. Build/Test function of DEMUX Digital IC

## V Relevant Affective Domain related outcome(s)

Significance of select lines to connect input data line to selected one output from many outputs.

Handle the component and equipment carefully.

Follow all safety precaution

## VI Relevant Theoretical Background

Demultiplexer has only one input and “n” number of outputs along with “m” number of select inputs. A demultiplexer performs the reverse operation of multiplexer i.e. it receives one input and distributes it over several outputs. At a time only one output line is selected by the select lines and the input is transmitted to the selected output line. Hence demultiplexer is equivalent to a single pole multiple way switch as shown in figure. The enable input will enable the demultiplexer. The relation between the n output lines and m select lines is as given below.

$$n=2^m$$

The demultiplexer performs opposite process to a multiplexing process it performs “one to many” operation. It has only one input (D) and n number of outputs (YO, Yl,Y2... Yn-1) as shown in the figure given below. Demultiplexer can also be used as a decoder e.g. Binary to Decimal Decoder. Data input given is I, strobe/enable pin issued for enabling DEMUX

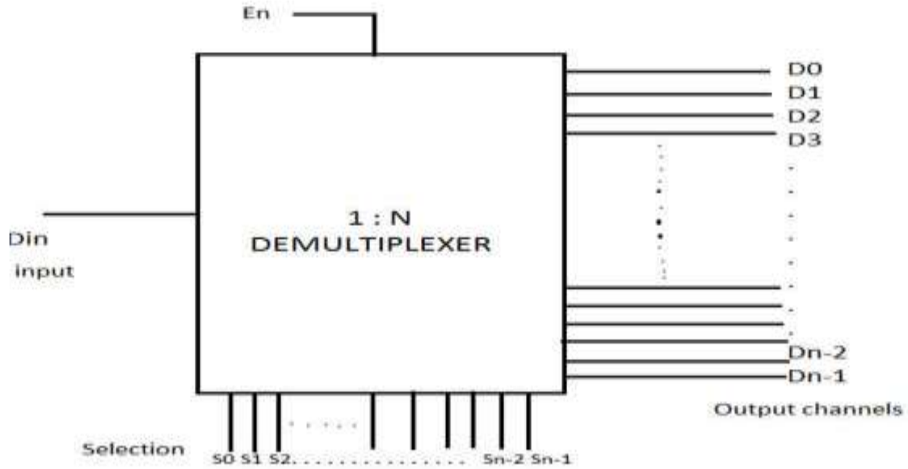


**Fig 11.1: Block diagram of 1: n Demultiplexer**

Curtesy: https://www.semiconductorforu.com/wp-content/uploads/2022/09/demultiplexer.jpg

**Types of Demultiplexer (DEMUX):**

1. 1:2 MUX (1 line to 2 lines)
2. 1:4 MUX (1 line to 4 lines)
3. 1:8 MUX (1 line to 8 lines)
4. 1:16 MUX (1 line to 16 lines)

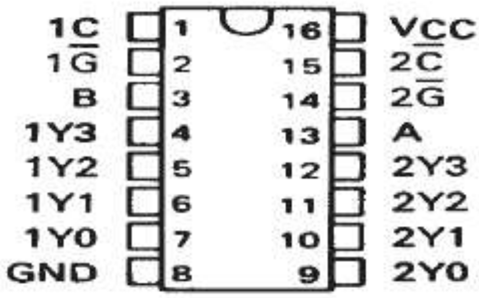


**Fig 11.2 IC SN74155 1:4 Demux**

Courtesy: https://www.digchip.com/datasheets/parts/datasheet/477/SN74155-pdf.php

**VII Circuit diagram**

**a) Sample circuit**

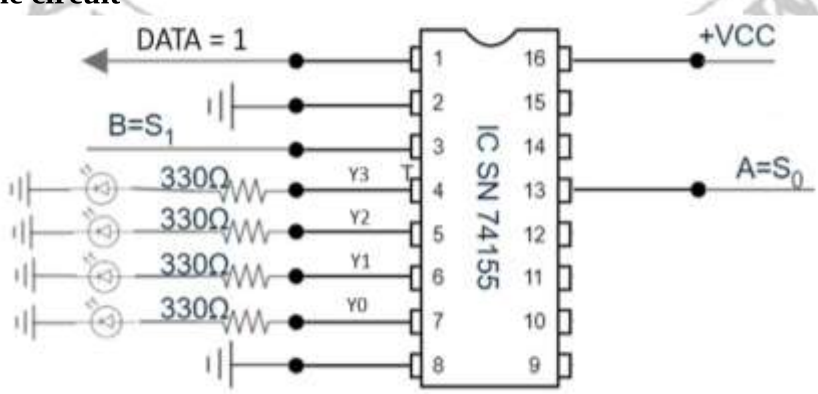


**Fig 11.3 Circuit Diagram of 1: 4 DEMUX using IC SN 74155**

(Note: Output of IC SN74155 is complementary to get desired output invert it by connecting NOT gate)

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC’s such as 74 series, 40/45 series of CMOS IC’s | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | SN74155 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 6( 2 for Select Lines and 4 for outputs) |
| 8 | Not gate | IC 7404 | 1 |
| 8 | Resistor | 220Ω/330Ω | 4 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Test the IC using Digital IC tester
2. Mount the IC on the breadboard
3. Make the connection as per fig 11.3.
4. Connect the +5V to +Vcc pin of IC and GND pin to ground
5. Connect the Strobe PIN $\overline{\mathbf{1G}}$ to ground.
6. Observe the LED (on or off) for each combination of input as per truth table
7. Verify the truth table

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure

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## XIII Observation:

**Table 11.1: Observation Table**

| Inputs | | | | Outputs | | | | Outputs (Volts) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Select | | Strobe $\overline{1G}$ | Data 1C | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
| B | A | | | | | | | | | | |
| X | X | 1 | X | | | | | | | | |
| 0 (0V) | 0 (0V) | 0 | 1 | | | | | | | | |
| 0 (0V) | 1 (5V) | 0 | 1 | | | | | | | | |
| 1 (5V) | 0 (0V) | 0 | 1 | | | | | | | | |
| 1 (5V) | 1 (5V) | 0 | 1 | | | | | | | | |

(Write the observation with respect to Inputs)

(Note: ‘X’ indicates the don’t care condition. It means the status of selected input may be any combination)

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are few sample questions for reference. Teacher must design more such questions so as to ensure the achievement of identifies CO.**

1. List the function of Strobe (G) pin?
2. List the name of manufacturers of IC'S used for this practical ?
3. Draw the Circuit diagram for 1:8 DeMUX using IC SN 74155 and its truth table?
4. State how DEMUX have helped for Data transfer in electronic circuits?

**[Space for Answers]**

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## XVIII References/Suggestions for further reading

1. https://www.digchip.com/datasheets/parts/datasheet/477/SN74155-pdf.php
2. https://www.youtube.com/watch?v=3aWLCH9_EPA (NPTEL Video Link on Demultiplexer)

## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| Marks Obtained | | | Dated signature of Teacher |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.12: Implement and verify the truth table of RS Flip-flop.**

**I Practical Significance**

A Flip-Flop is a basic digital logic circuit use for storing binary information. It is also known as One bit memory. It has two stable states typically 0 (reset) and 1 (set), and it can maintain its current state until it is instructed to change it by applying a clock pulse. Flip-Flops are fundamental building blocks in digital electronics, used in memory storage, sequential logic circuits and Data synchronization.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop sequential logic circuits using Flip-Flops.

**IV Laboratory Learning Outcome(s):**

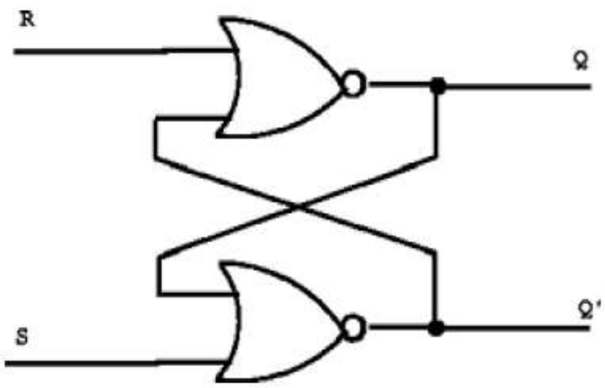
1. Build/Test functionality of RS flip flop using NAND Gate.

**V Relevant Affective Domain related outcome(s)**

Flip-Flop data holding/storing ability.
Handle the component and equipment carefully.
Follow all safety precaution

**VI Relevant Theoretical Background**

Digital circuits have many combinations of logic circuits. They are classified as either combinational or sequential. The output of combinational circuits depends only on the current inputs. In contrast, sequential circuit depends not only on the current value of the input but also upon the internal state of the circuit. Basic building blocks (memory elements) of a sequential circuit are the flip-flops (FFs). The FFs change their output state depending upon inputs at certain interval of time synchronized with some clock pulse applied to it.



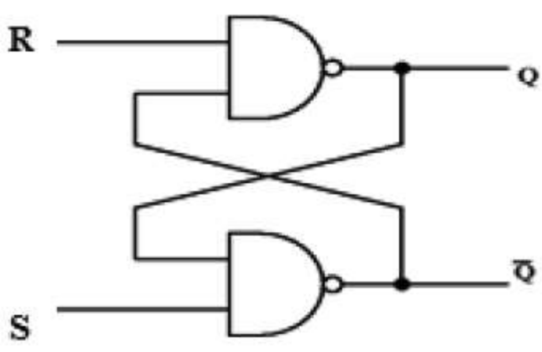




**Fig 12.1 a) SR latch using NOR gates** **b) SR latch using NAND gates**

| S | R | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | Same as previous | Same as previous |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Race | Race |

| S | R | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | Race | Race |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Same as previous | Same as previous |

**Fig 12.2 Truth table for Circuit diagram in Fig 12.1 a&b**

**VII Circuit diagram**

**a) Sample circuit**

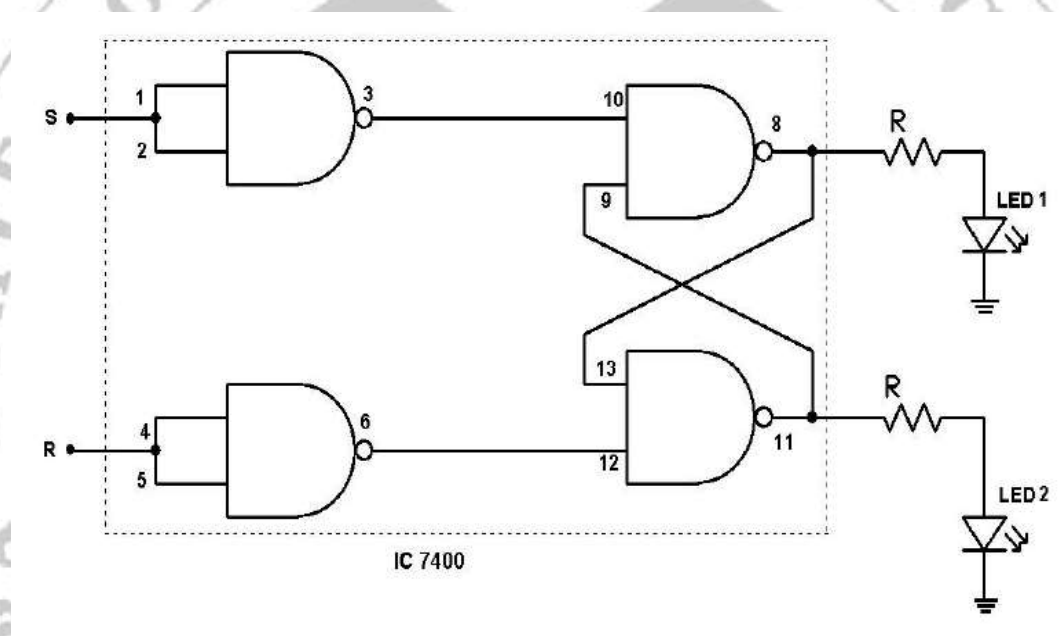



**Fig 12.3 SR Flip-Flop using NAND gates**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | 7400 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 2 |
| 8 | Resistor | 220Ω/330Ω | 4 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Mount the IC7400 on the breadboard.
2. Make the connections as shown in figure 12.3
3. Apply the supply voltage to IC +5V.
4. Apply inputs according to the observation table.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
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## XII Actual Procedure

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## XIII Observation:

**Table 12.1: Observation Table for SR Flip-Flop**

| Inputs | | Q | | $\bar{Q}$ | | Remark |
|---|---|---|---|---|---|---|
| S | R | Logic Level (0/1) | Output Voltage (V) | Logic Level (0/1) | Output Voltage (V) | |
| 0 (0V) | 0 (0V) | | | | | |
| 1 (5V) | 0 (0V) | | | | | |
| 0 (0V) | 1 (5V) | | | | | |
| 1 (5V) | 1 (5V) | | | | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are few sample questions for reference. Teacher must design more suchquestions so as to ensure the achievement of identifies CO.**

1. Why the Name of Flip-Flop is given SR Flip-Flop?
2. Explain the Race Condition in SR Flip-Flop?
3. List how race condition can be resolved?
4. State application of SR Flip-Flop?

**[Space for Answers]**

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**XVIII References/Suggestions for further reading**


1. https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/ (Virtual Lab Link on SR Flip-Flop)
2. https://www.youtube.com/watch?v=jm0PGDSSBkI (NPTEL Video Link on Latch and Flip-Flop (Part 1))
3. https://www.youtube.com/watch?v=i-tnQMDdbfc (NPTEL Video Link on Latch and Flip-Flop (Part 2))


**XIX Assessment Scheme**

| | **Performance Indicators** | **Weightage** |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.13: Implement and Test the functionality of Master Slave JK Flip Flop using Digital IC.**

**I Practical Significance**

The limitation of SR flip flop is overcome in JK flip flop. In JK flip flop when J=K=l, the output is uncertain; this situation is called Race around condition. To avoid the problem of race around condition the JK flip flop in Master and slave mode is used.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop sequential logic circuits using Flip-Flops.

**IV Laboratory Learning Outcome(s):**

1. Build/Test functionality of Master Slave (MS) JK flip flop using IC 7476.

**V Relevant Affective Domain related outcome(s)**

Handle the component and equipment carefully.

Follow all safety precaution

**VI Relevant Theoretical Background**

Master Slave J K flip flop is a cascade of two S-R flip-flops, with feedback from the outputs of the second flip flop to the inputs of the first. The first part is called as master flip-flop while the next is called as slave flip-flop .Here the master flip-flop is triggered by the external clock pulse while the slave is activated at its inversion i.e. if the master is positive level triggered, then the slave is negative-level triggered and vice-versa. This means that the data enters into the flip-flop at positive/negative level of the clock pulse while it is obtained at the output pins during positive/negative level of the clock pulse. Hence a master-slave flip-flop completes its operation only after the appearance of one full clock pulse.

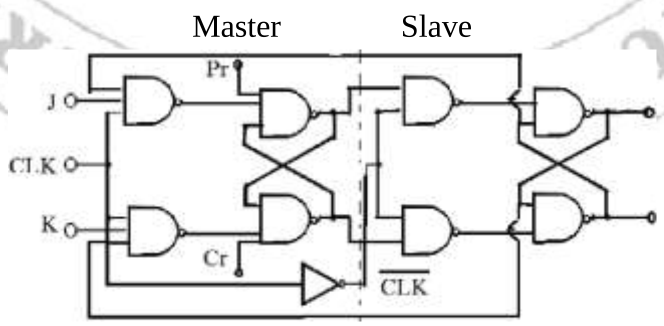
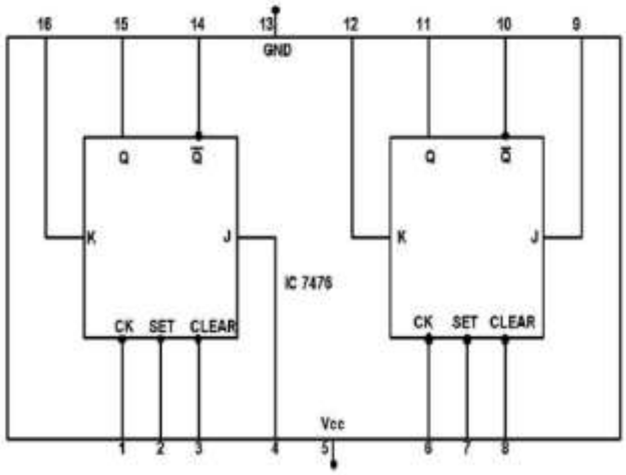



**Fig 13.1 Master Slave J-K flip flop**

## VII Circuit diagram

### a) Sample circuit



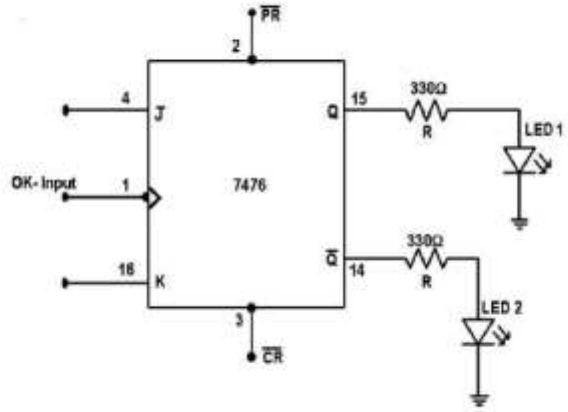




**Fig 13.2 a)Pin Configuration of IC 7476 b)Master Slave J-K flip flop**

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| **PR** | **CLR** | **CLK** | **J** | **K** | **Q** | $\overline{Q}$ |
| 1 | 1 | 1 | 0 | 0 | $Q_0$ | $\overline{Q}_0$ |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | Toggle | |

**Fig 13.3 Truth table for Circuit diagram in Fig 13.2 a & b**

### b) Actual circuit

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | DM7476 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 2 |
| 8 | Resistor | 220Ω/330Ω | 2 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Mount the IC7476 on the breadboard.
2. Make the connections as shown in figure 13.2b
3. Apply the supply voltage to IC +5V.
4. Apply inputs according to the observation table.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure

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## XIII Observation:

**Table 13.1: Observation Table for SR Flip-Flop**

| Inputs | | | | | Q | | $\overline{Q}$ | |
|---|---|---|---|---|---|---|---|---|
| PR | CLR | CLK | J | K | Logic Level (0/1) | Output Voltage (V) | Logic Level (0/1) | Output Voltage (V) |
| 1 | 1 | 1 | 0 (0V) | 0 (0V) | | | | |
| 1 | 1 | 1 | 1 (5V) | 0 (0V) | | | | |
| 1 | 1 | 1 | 0 (0V) | 1 (5V) | | | | |
| 1 | 1 | 1 | 1 (5V) | 1 (5V) | | | | |

Note: Logic 1=5V and Logic 0=0V

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are few sample questions for reference. Teacher must design more such questions so as to ensure the achievement of identifies CO.**

1. What is the significance of Master and Slave combination?
2. Explain the Race Condition is overcomed in MS JK Flip-Flop?
3. Toggle condition of MS JK is used where in Electronic application.?
4. List the manufacturers of MS JK Flip-Flop IC?

**[Space for Answers]**

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**XVIII References/Suggestions for further reading**

1. https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/ (Virtual Lab Link on JK Flip-Flop)
2. https://www.youtube.com/watch?v=T2ofdrTPqPw (NPTEL Video Link on Latch and Flip-Flop (Part 3))
3. https://www.alldatasheet.com/datasheet-pdf/pdf/50913/FAIRCHILD/7476.html

**XIX Assessment Scheme**

| Performance Indicators | | Weightage |
|---|---|---|
| **Process Related : 15 Marks** | | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| **Product Related: 10 Marks** | | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| **Total ( 25 Marks)** | | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.14: Use Digital IC to construct and Test the functionality of D and T Flip Flop.**

**I Practical Significance**

D Flip –Flop (Delay Flip –Flop) is used to provide time delay. They are basic building blocks of Shift Registers.

T Flip-Flop (Toggle Flip-Flop) experiences a change in output in each clock edge.

Hence it can be used as a frequency divider. T Flip-Flop can also be used to design Counters

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop sequential logic circuits using Flip-Flops.

**IV Laboratory Learning Outcome(s):**

1. Build/Test functionality and Truth Table of D and T flip flop.

**V Relevant Affective Domain related outcome(s)**

Handle the component and equipment carefully.

Follow all safety precaution

**VI Relevant Theoretical Background**

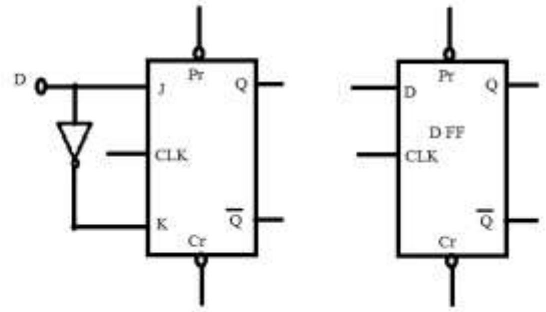
Flip-flops are fundamental building blocks in digital electronics, used for storing binary data. The D and T flip-flops are two common types, each with its unique characteristics and applications.

1. **D Flip-Flop (Data Flip-Flop):**
   - The D flip-flop has a single data input (D) and two outputs: Q (the stored value) and Q' (the complement of the stored value).
   - It changes its output state (Q) only when the clock input (CLK) transitions from a specific state to another (e.g., rising or falling edge).
   - The D input is sampled and stored when the clock transitions occur. Thus, the output reflects the state of the D input at the last clock transition.
   - D flip-flops are commonly used for data storage, synchronization, and edge detection in digital circuits.

2. **T Flip-Flop (Toggle Flip-Flop):**
   - The T flip-flop has a single input (T) called the toggle input, and two outputs: Q and Q'.
   - It toggles its output state (Q) based on the transition of the clock input (CLK) and the state of the toggle input (T).
   - When T is high (1), the output toggles (Q changes its state) on each clock transition.
   - When T is low (0), the output holds its state regardless of clock transitions.
   - T flip-flops find applications in frequency division, pulse generation, and digital

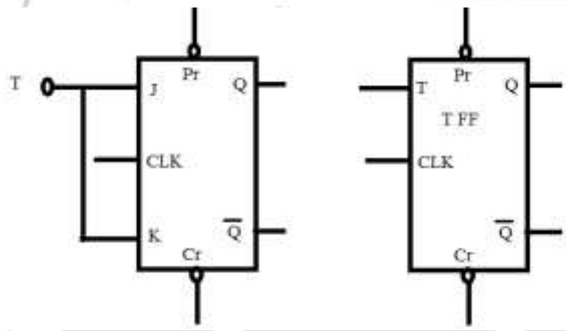
counters due to their toggling behavior.

In summary, The D flip-flop stores data and updates its output on clock transitions, while the T flip-flop toggles its output based on clock transitions and the state of its toggle input. Both are essential components in digital circuit design, offering versatility and functionality in various applications.




| Input D | Output $Q_{n+1}$ |
|---|---|
| 0 | 0 |
| 1 | 1 |

**Figure 14.1 a) D FF using 7476 b) Symbol c) Truth Table**




| Input T | Output $Q_{n+1}$ |
|---|---|
| 0 | $Q_n$ |
| 1 | $\overline{Q_n}$ |

**Figure 14.2 a) T FF using 7476 b) Symbol c) Truth Table**

**VII Circuit diagram**

**a) Sample circuit**

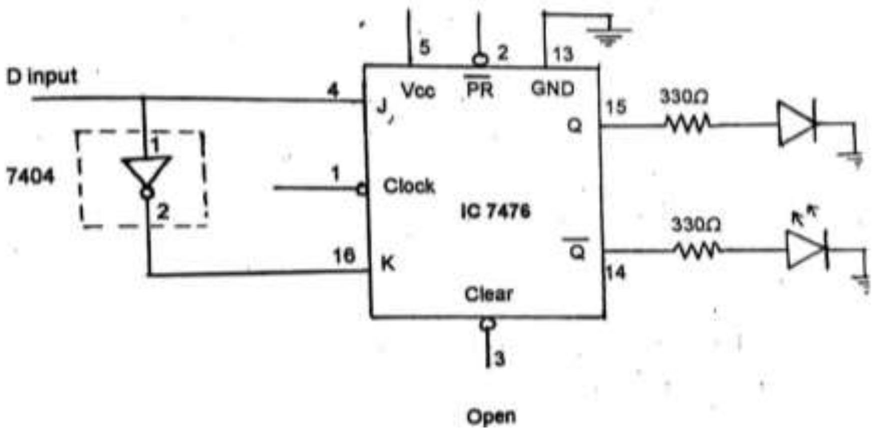



**Figure 14.3 D FF using 7476**

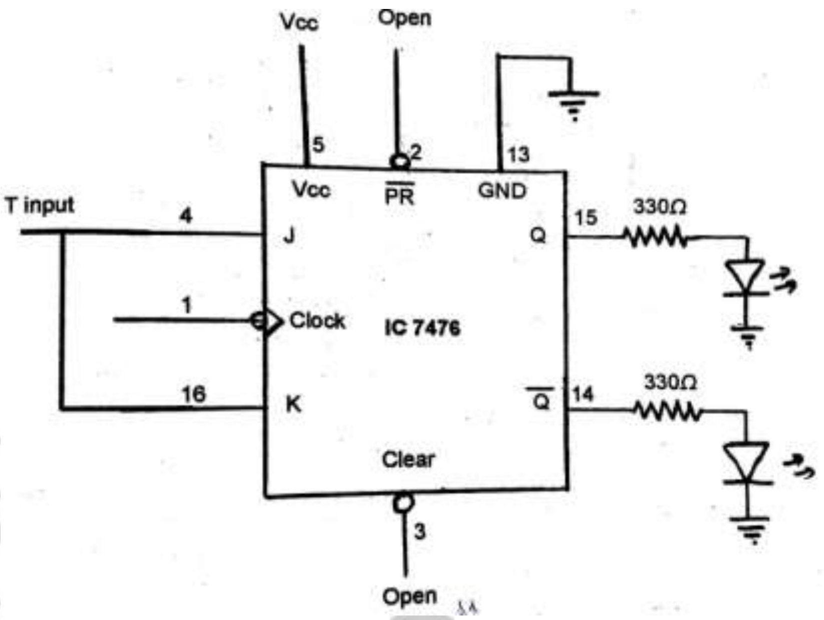



**Figure 14.4 T FF using 7476**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | DM7476 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 2 |
| 8 | Resistor | 220Ω/330Ω | 2 |

## IX Precautions to be followed

1. Check IC before use.
2. Set power supply to 5V (Variable DC Power Supply) before connecting.
3. Check all the connections as per circuit diagram

## X Procedure

1. Mount the IC7476 on the breadboard.
2. Make the connections as shown in figure 14.3 and 14.4
3. Apply the supply voltage to IC +5V.
4. Apply inputs according to the observation table.
5. Observe the LED (on or off) for each combination of input as per truth table.
6. Verify the truth table.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure:

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## XIII Observation:

**Table 14.1: Truth Table D, T flip-flop**

| **Input D** | **Output $Q_{n+1}$** | |
|---|---|---|
| | **Logic Level (0/1)** | **Output Voltage (V)** |
| **0 (0V)** | | |
| **1 (5V)** | | |

| **Input T** | **Output $Q_{n+1}$** | |
|---|---|---|
| | **Logic Level (0/1)** | **Output Voltage (V)** |
| **0 (0V)** | | |
| **1 (5V)** | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are few sample questions for reference. Teacher must design more suchquestions so as to ensure the achievement of identifies CO.**

1. Can T flip flop be used as frequency divider? Explain in 2 to 3 lines?
2. What is meaning of Toggle?
3. Different Types of Trigger used in D and Type of flip-flops
4. Mentioned the IC no. of D Flip-Flop and Draw its pin configuration?

**[Space for Answers]**

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## XVIII References/Suggestions for further reading

1. https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/ (Virtual Lab Link on D and T Flip-Flop)
2. https://www.youtube.com/watch?v=uadAVCbKx5Y (NPTEL Video Link )
3. https://www.alldatasheet.com/datasheet-pdf/pdf/50913/FAIRCHILD/7476.html

## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

## Practical No.15: Build 4-bit Universal Shift register and Observe the Timing diagram

**I Practical Significance**

Universal Shift Register is a register which can be configured to load and/or retrieve the data in any mode (either serial or parallel) by shifting it either towards right or towards left. In other words, a combined design of unidirectional (either right- or left-shift of data bits as in case of SISO, SIPO, PISO, PIPO) and bidirectional shift register along with parallel load provision is referred to as **universal shift register.**

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Develop sequential logic circuits using Flip-Flops.

**IV Laboratory Learning Outcome(s):**

1. Interpret timing diagram of 4 bit Universal shift register.

**V Relevant Affective Domain related outcome(s)**

Handle the component and equipment carefully.
Follow all safety precaution

**VI Relevant Theoretical Background**

A Universal shift register is a digital circuit that can shift data in either direction(left or right) and perform parallel-to-serial or Serial-to-Parallel conversion.It typically consist of a cascade of flip-flops interconnected to form a shift register, along with control logic to manage shifting operations

The key feature of a universal shift register is its versatility in handling various types of data manipulation tasks. It can shift data left or right based on control signals, enabling it to perform functions such as data storage, serial data transmission, serial data reception, parallel data loading, and parallel data retrieval.

Various control Functions in shift registers are as below.

1. A shift-right control to enable the shift-right operation and the serial input and output lines associated with the shift-right.
2. A shift-left control to enable the shift-left operation and the serial input and output lines associated with the shift-left.
3. A parallel-load control to enable a parallel transfer and the *n* input lines associated with the parallel transfer.
4. n parallel output lines.
5. A clear control to clear the register to 0.
6. A CLK input for clock pulses to synchronize all operations.

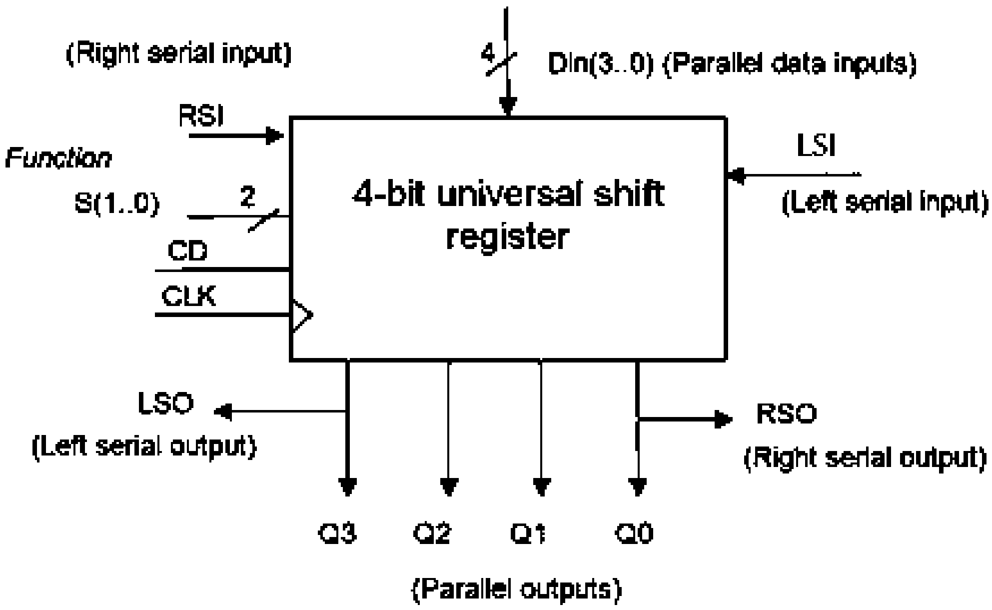


**Fig 15.1 Block Diagram of 4-bit Shift register.**

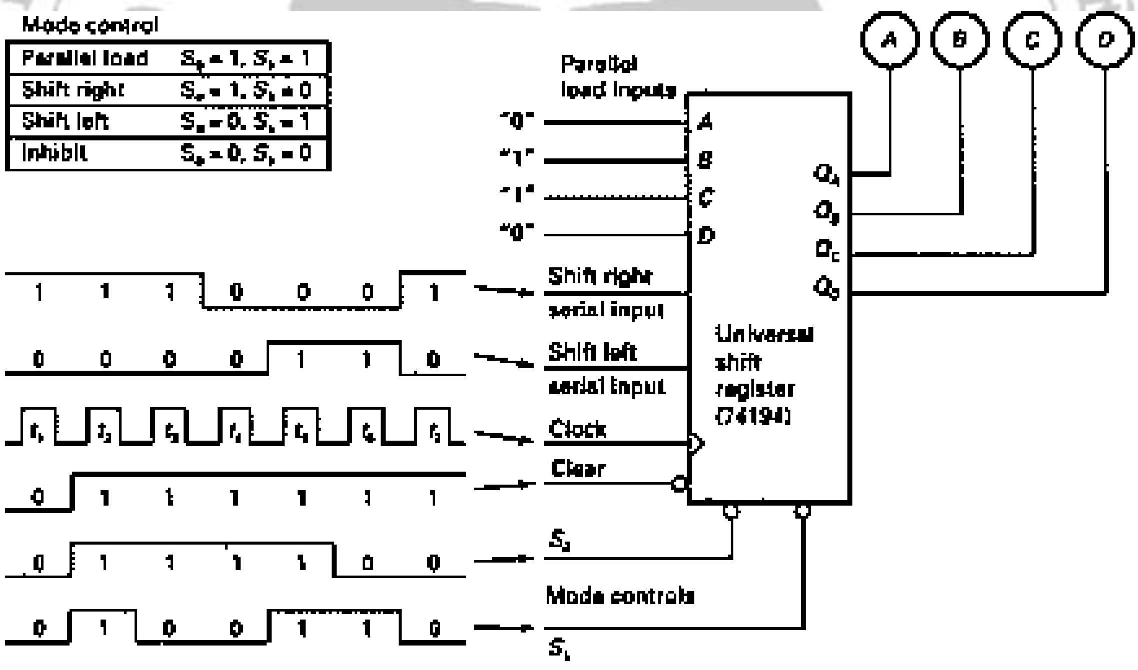


**Fig.15.2 Wiring Diagram for universal shift register using IC 74194**

Curtesy: https://www.transtutors.com/questions/power-off-rewire-the-74194-ic-to-form-a-parallel-load-shift-left-right-register-see--9128611.htm

## VII Circuit diagram

### a) Sample circuit

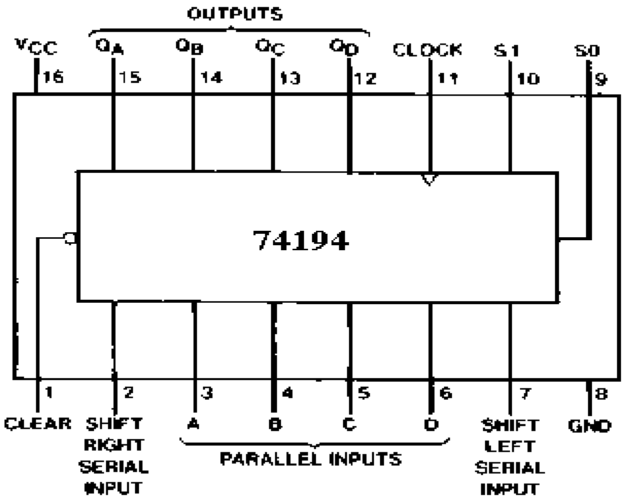


**Fig15.3 Sample ckt for 4 bit universal shift register using IC 74194.**

Students can use fig 15.2 also for connection. Reference no 7 in reference section can also be used for connection.

### b) Actual circuit

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | 74194 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 4 |
| 8 | Resistor | 220Ω/330Ω | 4 |
| 9 | Clock Pulse | Function/Pulse Generator | 1 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Connect appropriate resistor and LED to output Q.
2. Clear all the flip-flops by applying active low input to the clear pin so that the flip-flops have 0000 stored in them.
3. Apply clock pulse one by one to clock input.
4. Connect input and observe output for all modes.
5. Write down observation table

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
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## XII Actual Procedure:

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## XIII Observation:

**Observation Table 15.1: Serial in Serial out Right Shift Operation**

Data:-1010 or as student selects

| Clear | Mode | | CLK | Serial Right Data(SR) | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_0$ | | | | | | |
| 1 | 0 | 1 | ↑ | 1 | | | | |
| 1 | 0 | 1 | ↑ | 0 | | | | |
| 1 | 0 | 1 | ↑ | 1 | | | | |
| 1 | 0 | 1 | ↑ | 1 | | | | |

Make Similar Observation table for Serial in Serial out left Shift Operation (Mode $S_1$=1, $S_0$=1 ).Draw its timing diagram on graph paper

**Observation Table 15.2 : Parallel In Parallel Out (Parallel Loading)**

| Clear | Mode | | CLK | Input Data | | | | Output Data | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_0$ | | $D_A$ | $D_B$ | $D_C$ | $D_D$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| 1 | 1 | 1 | ↑ | 0 | 1 | 0 | 1 | | | | |
| 1 | 1 | 1 | ↑ | 1 | 1 | 0 | 0 | | | | |
| 1 | 1 | 1 | ↑ | | | | | | | | |
| 1 | 1 | 1 | ↑ | | | | | | | | |

Note : Students can use different data in empty data column. Draw observation tables timing diagram on graph paper

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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## XVII Practical related questions

**Note: Below given are few sample questions for reference. Teacher must design more suchquestions so as to ensure the achievement of identifies CO.**

1 State the operation for SIPO and PISO.
2 Draw observation table for above operation.
3. Build circuit for SIPO,, and PISO separately.
4 Draw timing diagram for SIPO.
5.Give one application of each register?

**[Space for Answers]**

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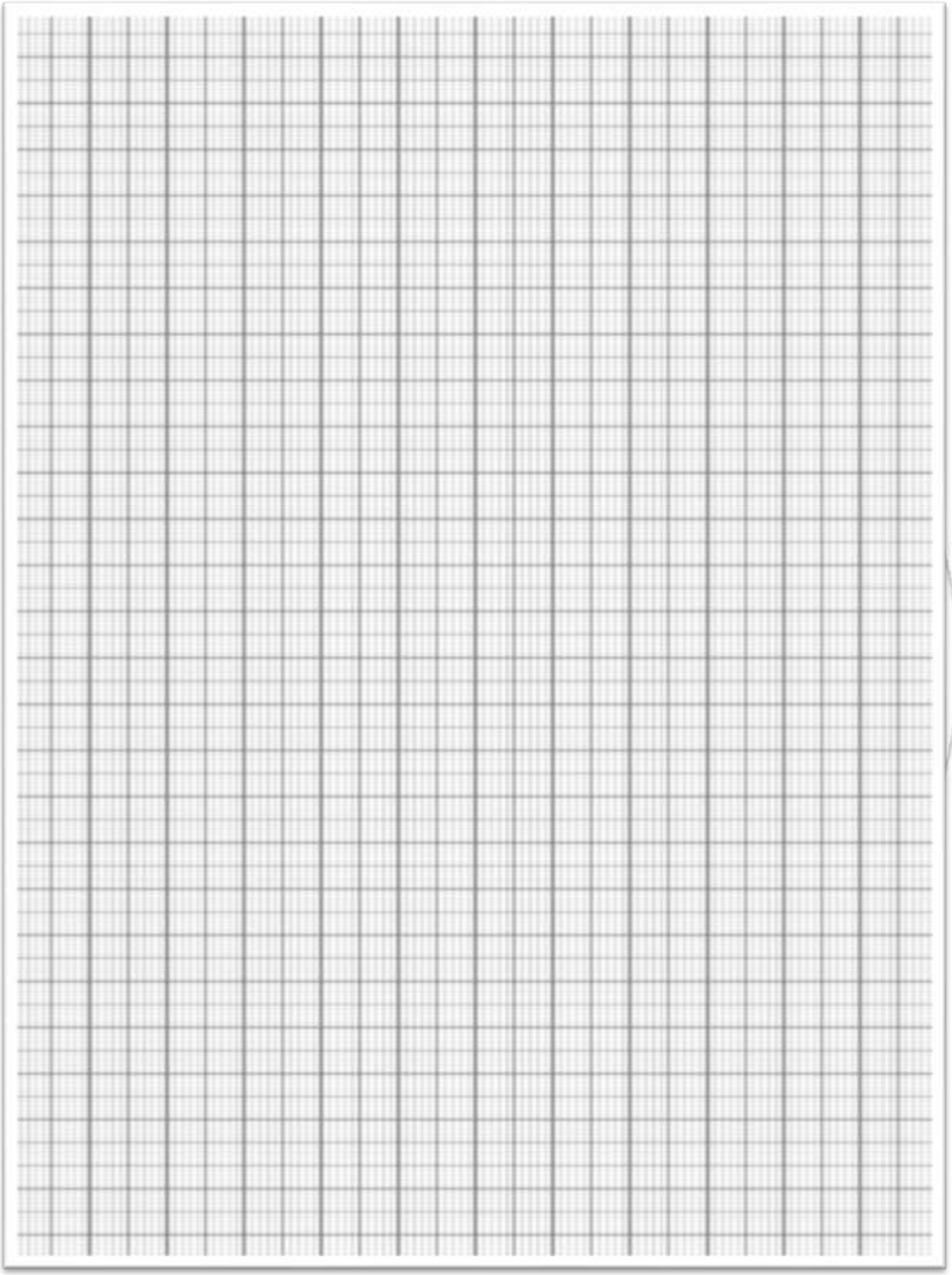
## XVIII References/Suggestions for further reading

1. https://he-coep.vlabs.ac.in/exp/shift-registers/index.html (Virtual Lab Link on Shift registers)
2. https://www.youtube.com/watch?v=ApILP5WPZeE (NPTEL Video Link )
3. www.sycelectronica.com.ar/semiconductores/74LS194.pdf

## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |



## Practical No.16: Implement Ripple Counter Using Digital IC

### I Practical Significance

In a ripple counter, each flip-flop stage is triggered by the output of the preceding stage. When the counter receives a clock pulse, the first flip-flop changes its state. This change in state causes a clock edge at the output of the first flip-flop, triggering the second flip-flop to change its state, and so on. The ripple effect propagates through the counter, with each subsequent flip-flop changing state in response to the change in state of the preceding flip-flop. As a result, ripple counters are inherently asynchronous, meaning that the timing of the clock pulses affects the overall operation and timing of the counter.

### II Industry/Employer Expected Outcome(s)

Students will be able to test the functionality of the digital circuits/system.

### III Course Level Learning Outcome(s)

Develop sequential logic circuits using Flip-Flops.

### IV Laboratory Learning Outcome(s):

1. Interpret timing diagram of 4 bit ripple counter using digital IC.

### V Relevant Affective Domain related outcome(s)

Handle the component and equipment carefully.
Follow all safety precaution

### VI Relevant Theoretical Background

In digital electronics, a counter is a sequential logic circuit that generates a sequence of binary numbers in a specified order. Counters are widely used in various applications such as frequency division, digital clocks, event counting, and addressing memory locations.
A counter typically consists of a set of flip-flops, where each flip-flop represents a binary digit (or "bit") of the counter's output. The number of flip-flops in the counter determines the maximum count that can be represented. For example, a counter with $n$ flip-flops can count up to $2^n$distinct states.

**There are different types of counters, including:**

Asynchronous (Ripple) Counters: In an asynchronous counter, the output of each flip-flop serves as the clock input for the next flip-flop. As a result, the flip-flops do not all change state simultaneously, leading to a ripple effect propagating through the counter. While simple to design, asynchronous counters suffer from longer propagation delays due to the ripple effect.

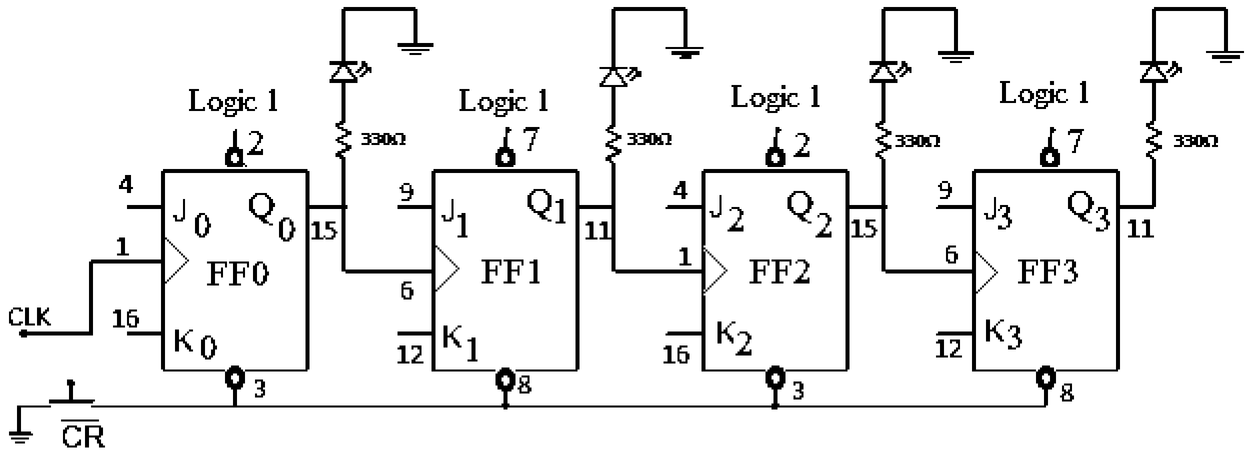
Synchronous Counters: In a synchronous counter, all flip-flops receive the same clock signal simultaneously. This ensures that all flip-flops change state simultaneously, eliminating the ripple effect and reducing propagation delays. Synchronous counters are often preferred for applications requiring precise timing.

Counters can also have additional features such as:

- Up Counters: Increment the count with each clock pulse.
- Down Counters: Decrement the count with each clock pulse.
- Bidirectional Counters: Count up or down based on control signals.
- Modulus Counters: Count up to a specific value before resetting.

**VII Circuit diagram**

**a) Sample circuit**




(J, K, PR terminals are kept open which act as high for TTL IC)

**Fig.16.1 bit Ripple Counter using J-K flip flop**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | 7476 | 2 |
| 7 | LED | Red/Yellow color 5 mm | 4 |
| 8 | Resistor | 220Ω/330Ω | 4 |
| 9 | Clock Pulse | Function/Pulse Generator | 1 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Connect +5V Power supply to proper pins of IC.
2. Connect appropriate resistor and LED to output Q.
3. Clear all the flip-flops by applying active low input to the clear pin so that the flip-flops have 0000 stored in them.
4. Apply clock pulse at clock input and after every clock pulse write down the counter output state from LED (ON LED =1 State, OFF LED =0 State)
5. Apply 16 clock pulses and write down the output of the counter in the truth table.

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure:

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## XIII Observation:

**Observation Table 16.1 : 4-BIT Asynchronous Up counter**

| Input | Output | | | | |
|---|---|---|---|---|---|
| **No. of clock pulses** | **$Q_3$** | **$Q_2$** | **$Q_1$** | **$Q_0$** | **Decimal Equivalent** |
| **0** | | | | | |
| **1** | | | | | |
| **2** | | | | | |
| **3** | | | | | |
| **4** | | | | | |
| **5** | | | | | |
| **6** | | | | | |
| **7** | | | | | |
| **8** | | | | | |
| **9** | | | | | |
| **10** | | | | | |
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| **12** | | | | | |
| **13** | | | | | |
| **14** | | | | | |
| **15** | | | | | |
| **16** | | | | | |

## XIV Result(s)

## XV Interpretation of results

## XVI Conclusion and recommendation

## XVII Practical related questions

**Note: Below given are few sample questions for reference. Teacher must design more such questions so as to ensure the achievement of identifies CO.**

1. Test output for Clear = 1 and Preset = 0.
2. What alteration in circuit will be done to convert 4 bit up counter in to 4 bit down counter?
3. Draw timing diagram for 4 bit Down counter?
4. How many flip-flop’s will be required to count 256 pulses?
5. Give three application of counters ?

**[Space for Answers]**

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**XVIII References/Suggestions for further reading**

1. https://he-coep.vlabs.ac.in/exp/shift-registers/index.html (Virtual Lab Link on counters/Refer refrence material for better understanding)
2. https://www.youtube.com/watch?v=WbNaLYJmBuk (NPTEL Video Link )

**XIX Assessment Scheme**

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

## Practical No.17: Implement Decade counter using digital IC

### I Practical Significance

Counter is a sequential circuit used for counting the number of clock pulses. It is a group of Flip-Flops with a clock signal applied to it. A counter has natural count of $2^n$ where "n" is number of flip-flop in the counter. Decade counter is a counter which has ten states from 0 to 9.

### II Industry/Employer Expected Outcome(s)

Students will be able to test the functionality of the digital circuits/system.

### III Course Level Learning Outcome(s)

Develop sequential logic circuits using Flip-Flops.

### IV Laboratory Learning Outcome(s):

1. Interpret timing diagram of Decade Counter (MOD-10).

### V Relevant Affective Domain related outcome(s)

Handle the component and equipment carefully.
Follow all safety precaution

### VI Relevant Theoretical Background

Decade counter is the one that goes through 10 unique combinations of output and then resets as the clock proceeds further. Since it is MOD -10 counters, it can be constructed with a minimum of four flip-flops. A four bit counter would have 16 states. By skipping any of six states by using some kind of feedback or some kind of additional logic, we can convert a normal four bit binary counter into a decade counter.

IC 7490 is a BCD asynchronous counter. It consists of 4 flip flops, internally connected so as to provide Mod-2 and Mod -5 counter functions. These ICs have set and reset inputs. These inputs help in designing a modulus –M counter. The Mod -2 and Mod -5 counters can be used independently or in combinations. Flip flop FFA operates as a mod-2 counter whereas the combination of flip flops FFB, FFC, and FFD form a mod-5 counter. There are two reset inputs R1 and R2 both of which are to be connected to logic 1 level to reset the flip flops. The two set inputs S1 and S2, when connected to logic 1 level, are used for setting the counter to 1001.for normal operation set and rest inputs are connected to 0.

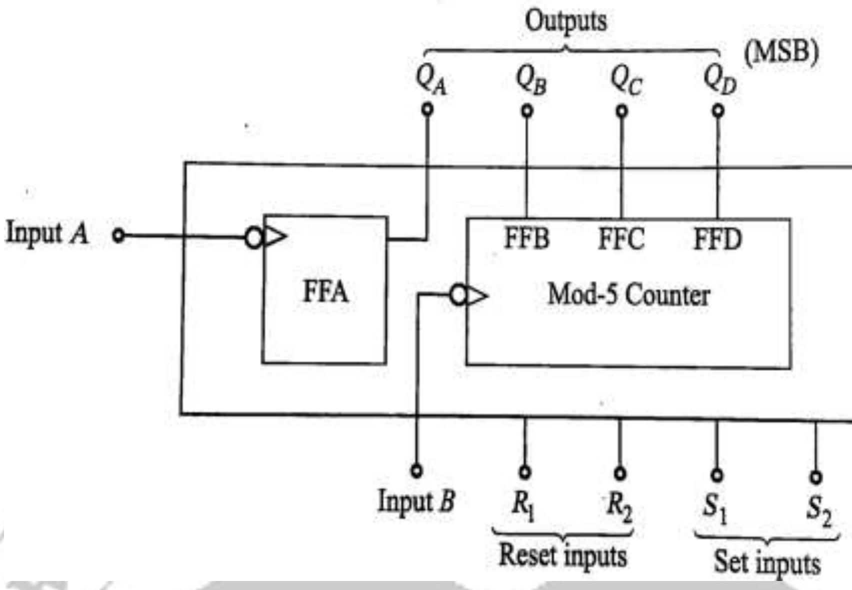


**Fig 17.1 Block diagram of IC 7490**

**VII Circuit diagram**

**a) Sample circuit**

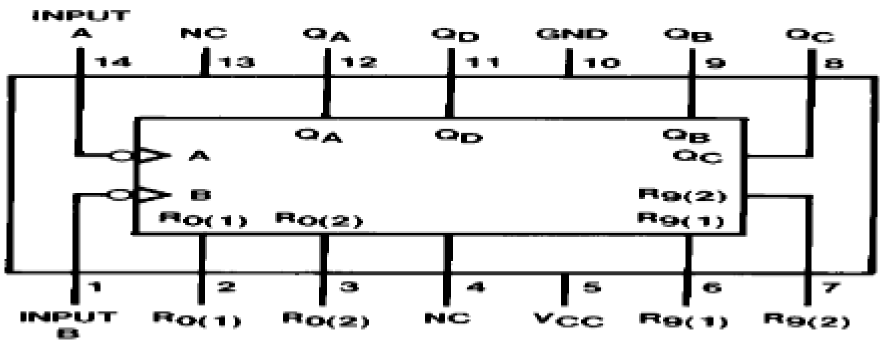


**Fig 17.2 Pin configuration of IC 7490**

Cutesy: https://pdf1.alldatasheet.com/datasheet-pdf/download/50915/FAIRCHILD/7490.html

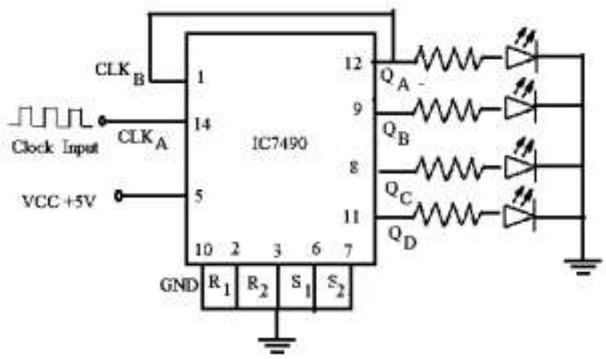


**Fig 17.3 Decade Counter using 7490**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Digital IC Tester | Tests a wide range of digital IC's such as 74 series, 40/45 series of CMOS IC's | 1 |
| 3 | DC Power supply | +5 V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | 7490 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 4 |
| 8 | Resistor | 220Ω/330Ω | 4 |
| 9 | Clock Pulse | Function/Pulse Generator | 1 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 5V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Mount IC 7490 on breadboard
2. Make the connection for given circuit diagram.(figure 17.3)
3. Apply the clock input.
4. Observe and record the outputs on LEDs (ON/OFF).

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
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## XII Actual Procedure:

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## XIII Observation:

**Observation Table17.1: Decade Counter**

| Input | Output | | | | |
|---|---|---|---|---|---|
| No. of clock pulses | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ | Decimal Equivalent |
| 0 | | | | | |
| 1 | | | | | |
| 2 | | | | | |
| 3 | | | | | |
| 4 | | | | | |
| 5 | | | | | |
| 6 | | | | | |
| 7 | | | | | |
| 8 | | | | | |
| 9 | | | | | |
| 10 | | | | | |

## XIV Result(s)

## XV Interpretation of results

## XVI Conclusion and recommendation

## XVII Practical related questions

**Note: Below given are few sample questions for reference. Teacher must design more such questions so as to ensure the achievement of identifies CO.**

1. What will be the output if pin no. 2 R1 is connected to logic 1
2. Draw mod-2 counter using IC 7490.
3. How many clock pulses are required for MOD 9 counter?

**[Space for Answers]**

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**XVIII References/Suggestions for further reading**


1. https://he-coep.vlabs.ac.in/exp/shift-registers/index.html (Virtual Lab Link on counters/Refer refrence material for better understanding)
2. https://www.youtube.com/watch?v=gAotbVkEFe8 (NPTEL Video Link )
3. https://pdf1.alldatasheet.com/datasheet-pdf/download/50915/FAIRCHILD/7490.html


**XIX Assessment Scheme**

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| Marks Obtained | | | Dated signature of Teacher |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |

**Practical No.18: Test the output of given R-2R type Digital to Analog Converter for the given input.**

**I Practical Significance**

A digital to analog converter (DAC) is a circuit that converts digital numbers into analog voltage or current output. R-2R ladder is a resistive network of which output voltage is a properly weighted sum of the digital inputs. With this experiment you will get an exposure to R-2R network which is used in digital to analog converters.

**II Industry/Employer Expected Outcome(s)**

Students will be able to test the functionality of the digital circuits/system.

**III Course Level Learning Outcome(s)**

Interpret the functions of data converters and memories in digital electronic systems.

**IV Laboratory Learning Outcome(s):**

1. Build R-2R resistive network on breadboard to convert given digital data into analog.

**V Relevant Affective Domain related outcome(s)**

Identify PIN configuration of IC.
Handle the component and equipment carefully.
Follow all safety precaution

**VI Relevant Theoretical Background**

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin’s theorem in arriving at the desired output voltages. The R-2R network consists of resistors with only two values - R and 2R. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. This is elaborated in fig.18.1.

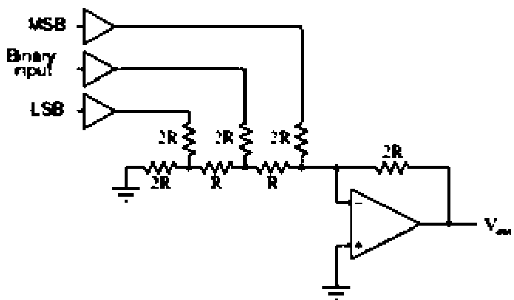


**Fig 18.1: Basic diagram of R-2R ladder network working of R-2R ladder network DAC**

- R-2R weighted resistor ladder network uses only 2 set of resistors R and 2R. If you want to build a very precise DAC, be precise while choosing the values of resistors that will exactly match the R-2R ratio.

- This is a 4bit DAC. Let us consider the digital data $D_3D_2D_1D_0$=0001 is applied to DAC, then the Thevenin's equivalent circuit reduction is shown below.

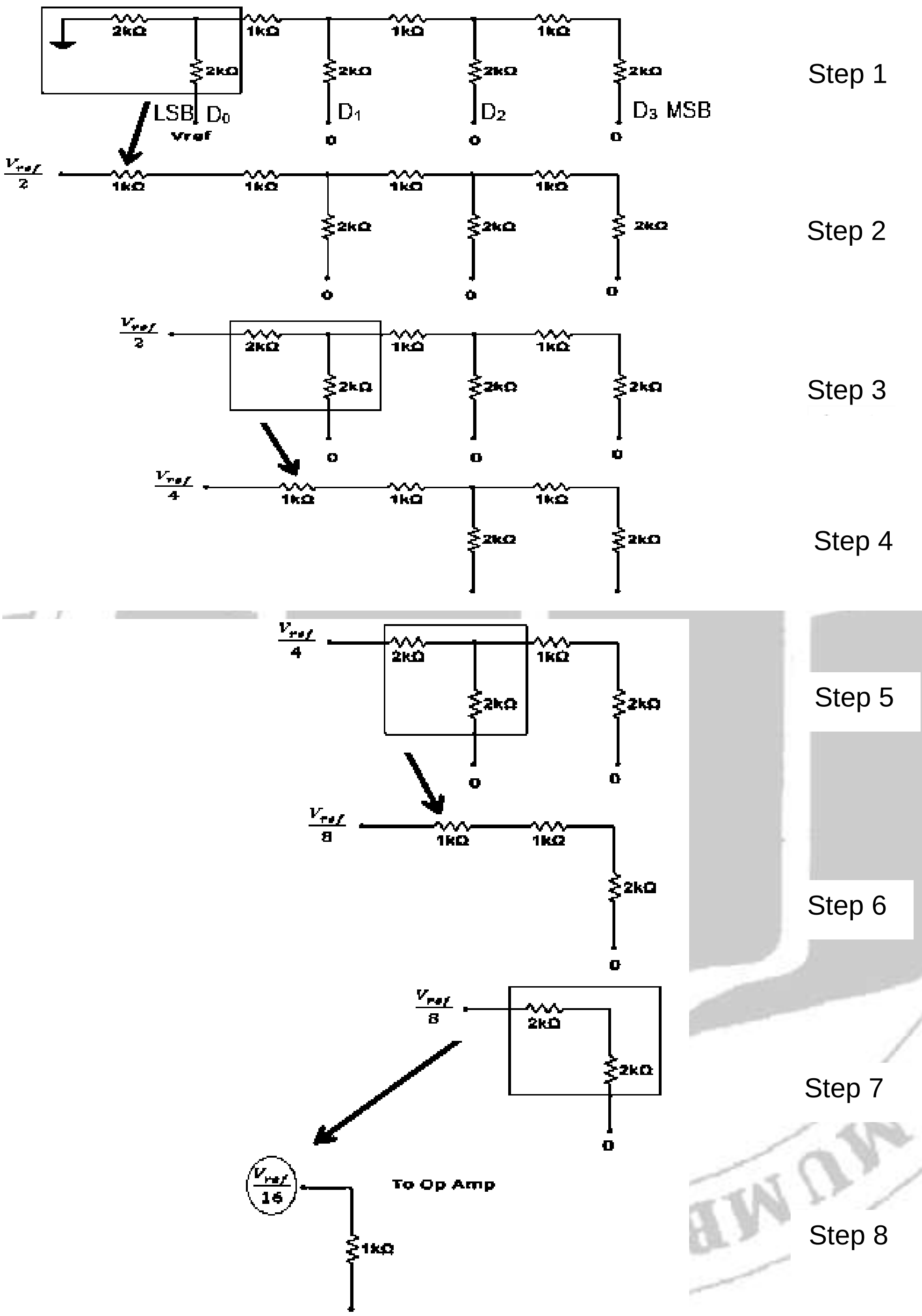


**Fig 18.2: Basic diagram of R-2R ladder network working of R-2R ladder network DAC**

- Vref is nothing but the input binary value reference voltage, that is for binary 1, Vref =5V and for binary 0, Vref =0V.

- For 0001 only D0=Vref, all other inputs are at 0V and can be treated as ground. So finally Vref/16 volt is appearing as the input to op amp. This value gets multiplied by the gain of op amp circuit – (Rf/Ri).
- If we proceed in this manner (Thevenin equivalent reduction), we will get

$$V_{out} = -\frac{R_f}{R_i} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2}\right]$$

- Note that you can build a DAC with any number of bits you want, by simply enlarging the resistor network, by adding more R-2R resistor branches.

**VII Circuit diagram**

**a) Sample circuit**

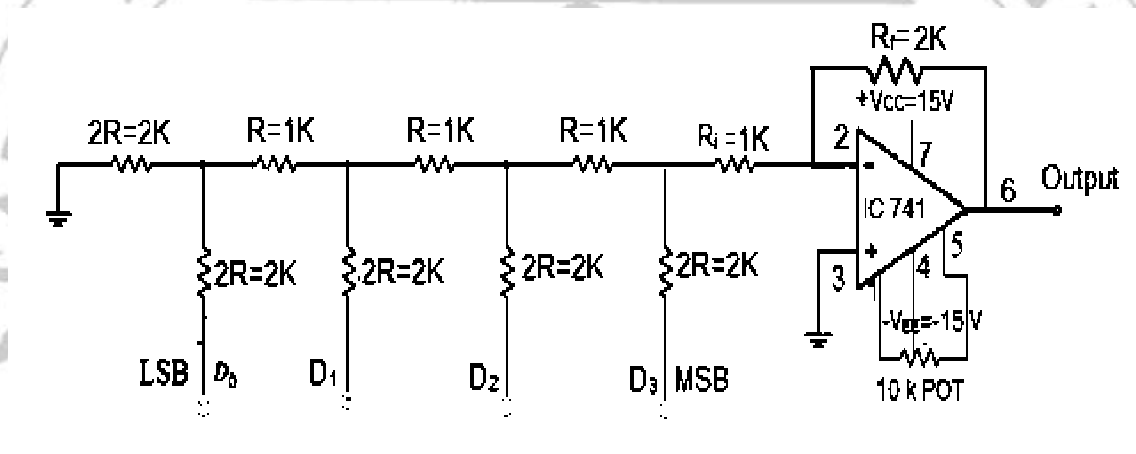


**Fig 18.3 R-2R Ladder DAC Network**

**b) Actual circuit**

## VIII Resources Required

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | Digital Multimeter | 3 ½ digit display | 1 or 2 |
| 2 | Analog IC Tester | Tests a wide range of Analog IC's | 1 |
| 3 | DC Dual Power supply | ±15V fixed power supply or Variable DC power supply (0-30V) | 1 |
| 4 | Breadboard | 5.5cm X 17cm | 1 |
| 5 | Connecting Wires | Single strand wires of 0.6 mm | As per Requirement |
| 6 | IC | 741 | 1 |
| 7 | LED | Red/Yellow color 5 mm | 2 |
| 8 | Resistor | 1KΩ and 2KΩ | 6 (2 KΩ)<br>4 (1KΩ) |
| 9 | Potentiometer | 10 KΩ | 1 |

## IX Precautions to be followed

1) Check IC before use.
2) Set power supply to 15V (Variable DC Power Supply) before connecting.
3) Check all the connections as per circuit diagram

## X Procedure

1. Test IC using IC tester.
2. Mount IC on bread board.
3. Build circuit as per circuit diagram.
4. Write down observation table.
5. With all inputs ($D_0$ to $D_3$) shorted to ground($D_0$=0,$D_1$=0,$D_2$=0,$D_3$=0), adjust the 10KΩ POT until the output is 0V.This will nullify any offset voltage at the input of the OPAMP.(POT connected between pin 1& pin 5 of OP-AMP)
6. Measure the output voltage for all binary input states.(0000 to 1111).

## XI Resources Used

| Sr. No. | Name of Resource | Suggested Broad Specification | Quantity |
|---|---|---|---|
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |

## XII Actual Procedure:

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## XIII Observation:

**Observation Table for R-2R Ladder DAC:**

| D3 | D2 | D1 | D0 | R-2R Ladder DAC | |
|---|---|---|---|---|---|
| | | | | Theoretical (V) $V_0 = -\frac{R_f}{R_i} * V_{ref}\left(\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2}\right)$ | Practical(V) |
| 0 | 0 | 0 | 0 | | |
| 0 | 0 | 0 | 1 | | |
| 0 | 0 | 1 | 0 | | |
| 0 | 0 | 1 | 1 | | |
| 0 | 1 | 0 | 0 | | |
| 0 | 1 | 0 | 1 | | |
| 0 | 1 | 1 | 0 | | |
| 0 | 1 | 1 | 1 | | |
| 1 | 0 | 0 | 0 | | |
| 1 | 0 | 0 | 1 | | |
| 1 | 0 | 1 | 0 | | |
| 1 | 0 | 1 | 1 | | |
| 1 | 1 | 0 | 0 | | |
| 1 | 1 | 0 | 1 | | |
| 1 | 1 | 1 | 0 | | |
| 1 | 1 | 1 | 1 | | |

## XIV Result(s)

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## XV Interpretation of results

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## XVI Conclusion and recommendation

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**XVII Practical related questions**

**Note: Below given are few sample questions for reference. Teacher must design more suchquestions so as to ensure the achievement of identifies CO.**

1 Define resolution of DAC.
2 State the purpose of op-amp in this circuit?
3 Write the steps to nullify any offset voltage at the input of the OPAMP.
4 Write down effect of number of input bits on output of DAC?
5 ……………………………………………………………………………………………

**[Space for Answers]**

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## XVIII References/Suggestions for further reading

1. http://vlabs.iitkgp.ac.in/psac/newlabs2020/vlabiitkgpAE/exp10/index.html#
   (Virtual Lab Link R-2R DAC)
2. https://www.youtube.com/watch?v=LUMhObAm1Qs (NPTEL Video Link )
3. https://datasheetspdf.com/datasheet-pdf/1463096/IC741.html

## XIX Assessment Scheme

| | Performance Indicators | Weightage |
|---|---|---|
| | **Process Related : 15 Marks** | **60 %** |
| 1 | Handling of the components | 10% |
| 2 | identification of components | 20% |
| 3 | Measuring value using suitable instrument | 20% |
| 4 | working in teams | 10% |
| | **Product Related: 10 Marks** | **40%** |
| 5 | Calculated theoretical values of given component | 10% |
| 6 | Interpretation of result | 05% |
| 7 | Conclusion | 05% |
| 8 | Practical related questions | 15% |
| 9 | Submitting the journal in time | 05% |
| | **Total ( 25 Marks)** | **100 %** |

| **Marks Obtained** | | | **Dated signature of Teacher** |
|---|---|---|---|
| **Process related (15)** | **Product related (10)** | **Total (25)** | |
| | | | |